
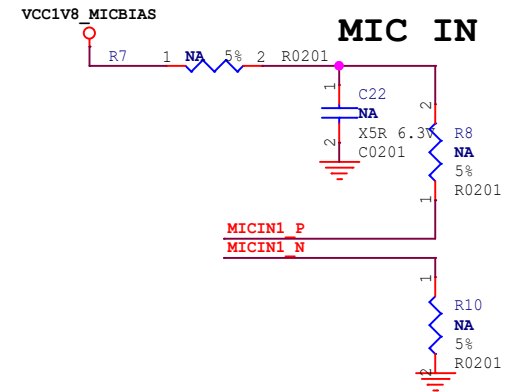
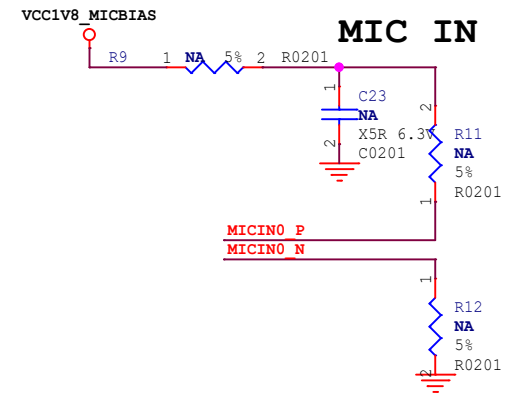
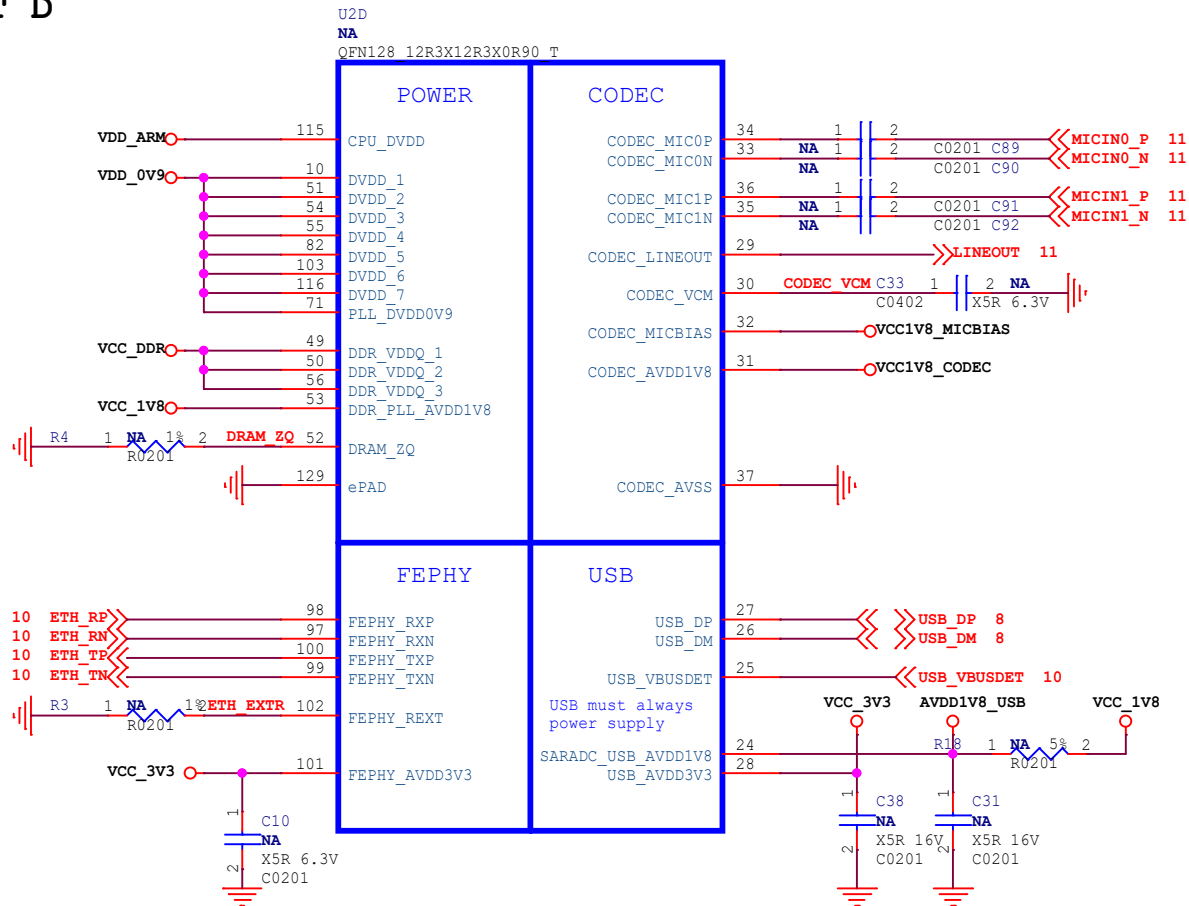


# RV1106G\_GMF\_V1.0

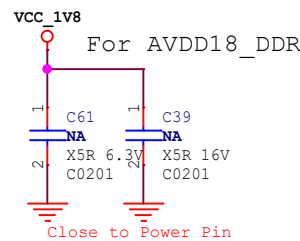
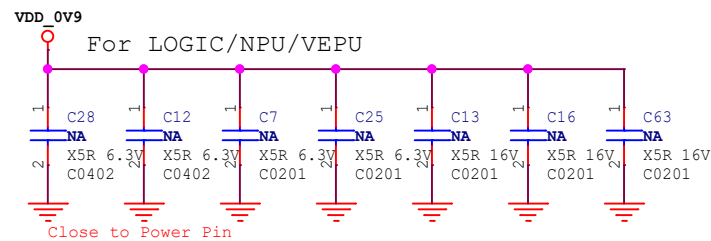
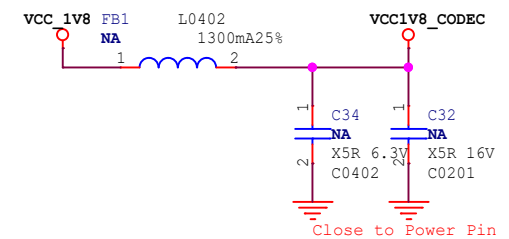
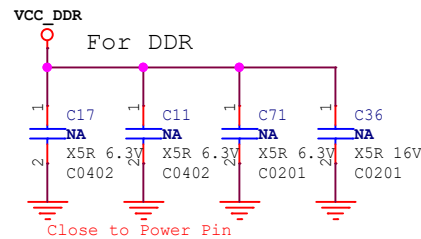
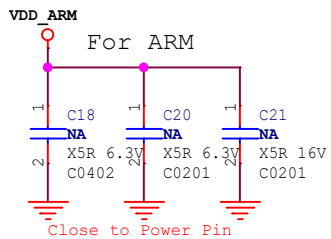
Reference Design Main Functions Introduction	
Power	Discrete
RAM	SPI FLASH
Interface	SDMMC/SDIO/MIPI_CSI/I2S/USB/ADC

HINLINK			
Project:	SoloLinker-A	 HINLINK	
File:	01.Cover Page		
Date:	Friday, August 02, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	1 of 12

# PART D



# POWER

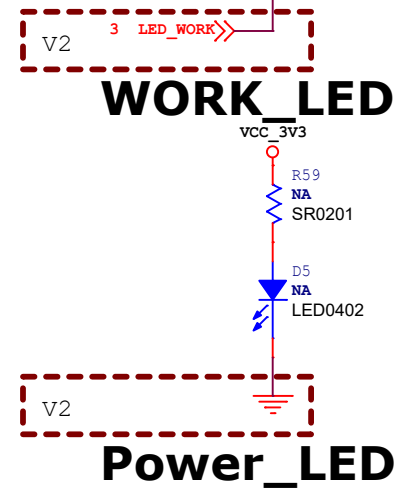
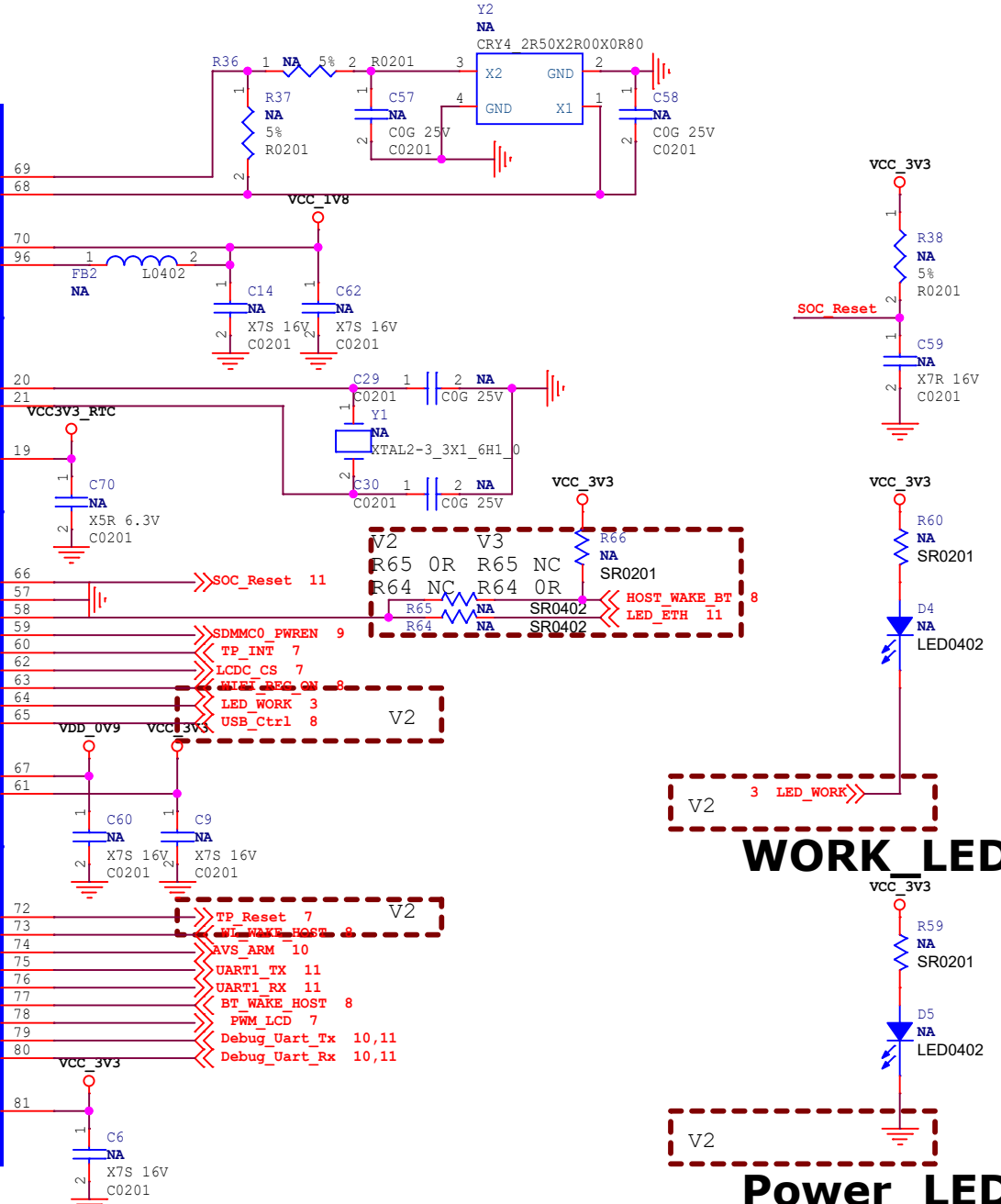
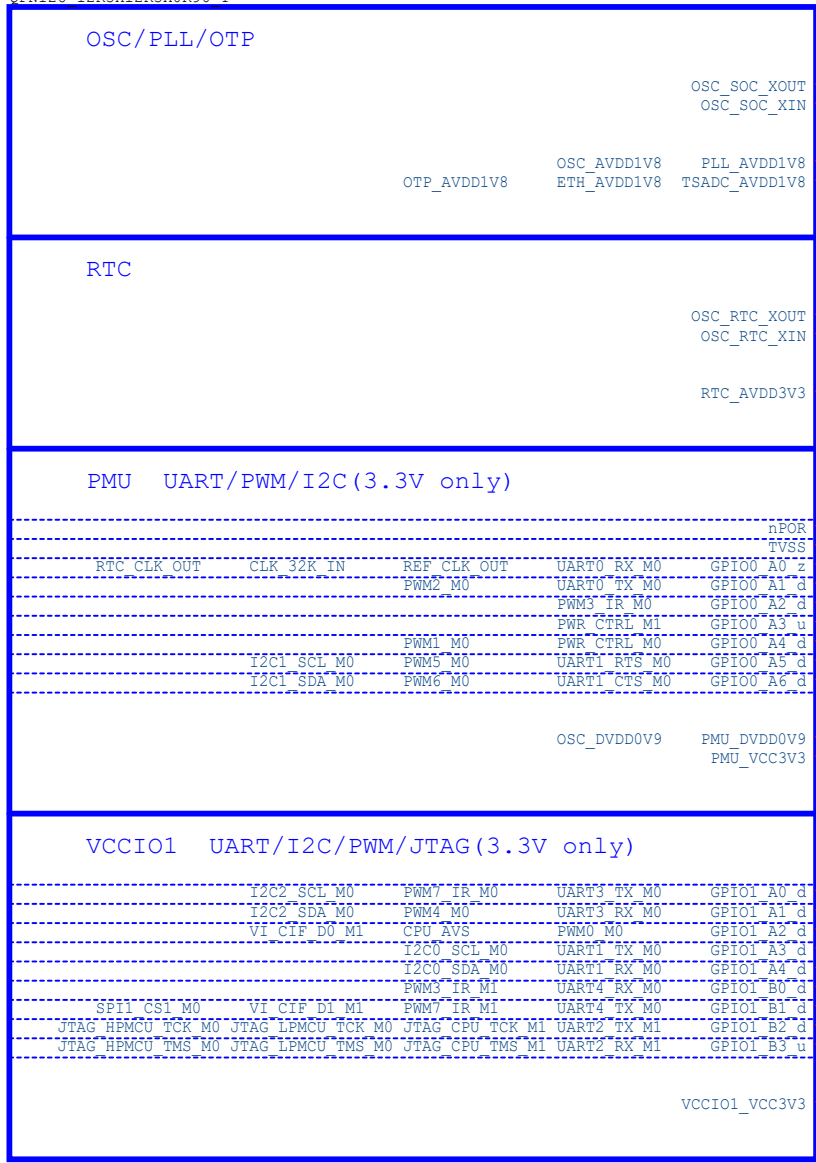


# HINLINK

<b>Project:</b>	SoloLinker-A	
<b>File:</b>	02.RV1106G Power/Codec/ETH/USB	
<b>Date:</b>	Saturday, November 02, 2024	<b>Rev:</b> <Revision>
<b>Designer:</b>	<designer>	<b>Sheet:</b> 2 of 12

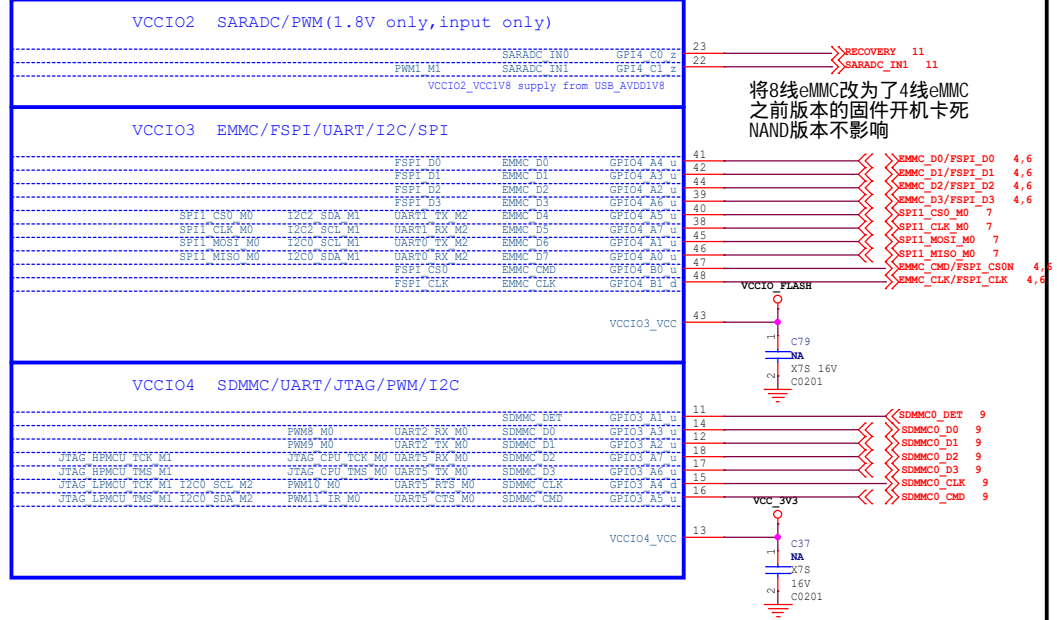
# PART A

U2A  
NA  
QFN128 12R3X12R3X0R90 T



<b>HINLINK</b>		
Project:	SoloLinker-A	
File:	03.RV1106G OSC/RTC/PMU/VCCIO	
Date:	Saturday, November 02, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 3 of 12

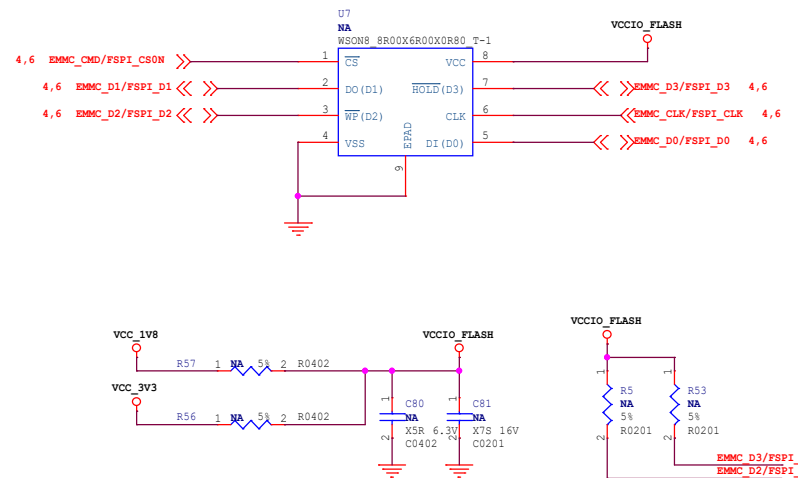
U2B  
NA  
GPN128 12R3X12R3X0R90 T



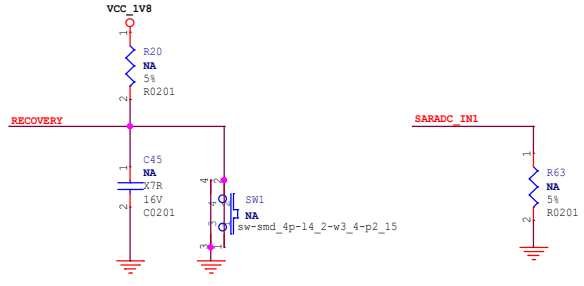
将8线eMMC改为了4线eMMC  
之前版本的固件开机卡死  
NAND版本不影响

SPI Flash

NOTE:  
Refer to the latest AVL for parts selection.



SARADC

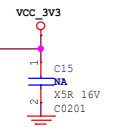


HINLINK			
Project:	SoloLinker-A	Rev:	<Revision>
File:	04.RV1106G ADC/FLASH/SDMMC	Sheet:	4 of 12
Date:	Saturday, November 02, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	4 of 12

U2C  
NA  
QFN128 12R3X12R3X0R90 T

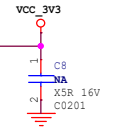
VCCIO5 SDIO/I2S/VO\_LCDC/UART/PWM/I2C

1204 SCL M0	UART1 RTS M1	VO_LCDC_D9	1230 LRCK	SDIO_D0 M0	GPIO2_X1 M1	110	>>	LCDC_D9	7
1204 SDA M0	UART1 CTS M1	VO_LCDC_D8	1230 SCLK	SDIO_D1 M0	GPIO2_X0 M1	109	>>	LCDC_D8	7
	UART1 RX M1	VO_LCDC_D7	1230 SDIO	SDIO_D2 M0	GPIO2_X5 M1	114	>>	LCDC_D13	7
		VO_LCDC_D6				113	>>	LCDC_D12	7
		VO_LCDC_D5				111	>>	LCDC_D10	7
		VO_LCDC_D4				112	>>	LCDC_D11	7
FLASH TRIGOUT	1203 SCL M0	PWM2 M1	1230 SD03 SD11	SDIO_CMD M0	GPIO2_X3 M1	107	>>	LCDC_D14	7
		VO_LCDC_D4	1230 SD02 SD12	UART0 RTS M1	GPIO2_A6 M1	106	>>	LCDC_D14	7
BREELIGHT TRIGOUT	1203 SDA M0	PWM4 M1	1230 SD01 SD13	UART0 CTS M1	GPIO2_A7 M1	105	>>	LCDC_D15	7
		VO_LCDC_D5				104	>>	LCDC_D16	7
		VO_LCDC_D6	1201 SCL M1	UART0 RX M1	GPIO2_B0 M1	104	>>	LCDC_D17	7
		VO_LCDC_D7	1201 SDA M1	UART0 TX M1	GPIO2_B1 M1				



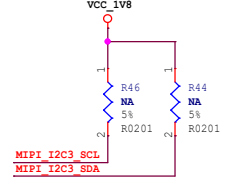
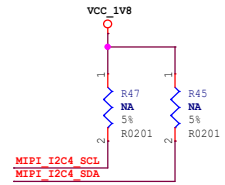
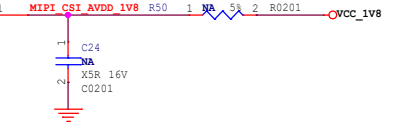
VCCIO6 VO\_LCDC/VI\_CIF/PWM/UART/I2C/SDIO/SPI/AUD\_DSM/VI\_BT656

VI_BT656_D0 M1	SDIO_D1 M1	SPI0_CS0 M0	PWM2 M2	VI_CIF_D3 M1	VO_LCDC_D7	GPIO1_C0 M1	95	>>	LCDC_D7	7		
VI_BT656_D1 M1	SDIO_D0 M1	SPI0_CLK M0	PWM4 M2	VI_CIF_D3 M1	VO_LCDC_D6	GPIO1_C1 M1	94	>>	LCDC_D6	7		
VI_BT656_D2 M1	1204 SCL M1	SDIO_CLK M1	SPI0_MOSI M0	PWM5 M2	VI_CIF_D4 M1	VO_LCDC_D5	GPIO1_C2 M1	92	>>	LCDC_D5	7	
VI_BT656_D3 M1	1204 SDA M1	SDIO_CMD M0	SPI0_MISO M0		VI_CIF_D5 M1	VO_LCDC_D4	GPIO1_C4 M1	91	>>	LCDC_D4	7	
VI_BT656_D4 M1		SDIO_D3 M1	UART0 RX M1	PWM6 M2	VI_CIF_D6 M1	VO_LCDC_D3	GPIO1_C5 M1	90	>>	LCDC_D3	7	
VI_BT656_D5 M1		SDIO_D2 M1	UART0 TX M1	PWM8 M1	VI_CIF_D7 M1	VO_LCDC_D2	GPIO1_C6 M1	89	>>	LCDC_D2	7	
VI_BT656_D6 M1		SDIO_D1 M1	UART1 RTS M1	PWM10 M1	VI_CIF_D8 M1	VO_LCDC_D1	GPIO1_C6 M1	88	>>	LCDC_D1	7	
VI_BT656_D7 M1		SDIO_D0 M1	UART1 CTS M1	PWM11 M1	VI_CIF_D9 M1	VO_LCDC_D0	GPIO1_C7 M1	89	>>	LCDC_D0	7	
VI_BT656_CLK M1			UART0 RX M1	PWM3 M2	VI_CIF_CLKI M1	VO_LCDC_DEN	GPIO1_D0 M1	87	>>	LCDC_DEN	7	
			UART0 TX M1	UART0 CTS M1	PWM10 M2	VI_CIF_HREF M1	VO_LCDC_HSYNC	GPIO1_B1 M1	86	>>	LCDC_HSYNC	7
SDIO_CS1 M0	1203 SDA M1	ADD_DSM_F	UART0 RX M1	PWM0 M2	VI_CIF_VSYNC M1	VO_LCDC_VSYNC	GPIO1_D2 M1	86	>>	LCDC_VSYNC	7	
SDIO_CS2 M0	1203 SCL M1	ADD_DSM_N	UART0 TX M1	PWM1 M2	VI_CIF_CLKO M1	VO_LCDC_CLK	GPIO1_D3 M1	85	>>	LCDC_CLK	7	



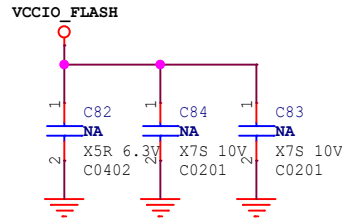
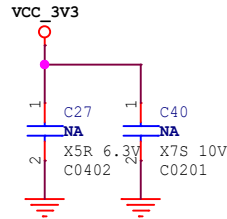
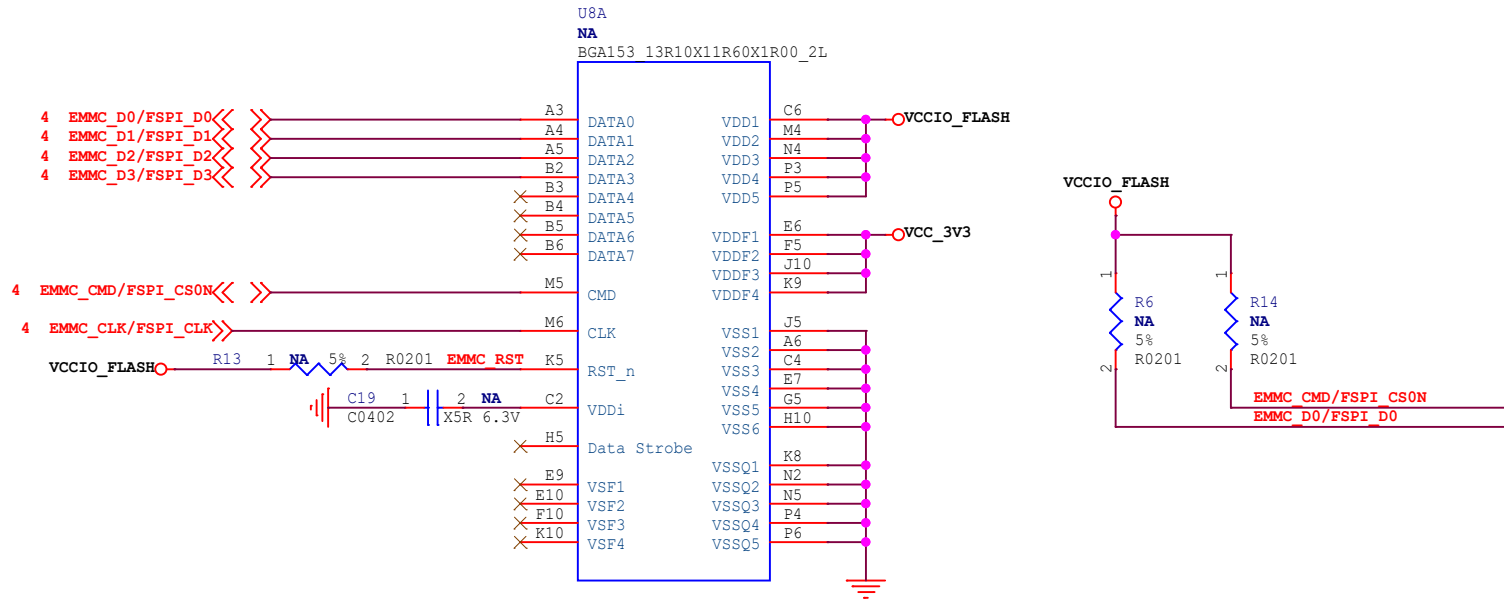
VCCIO7 VI\_CIF/MIPI CSI/LVDS RX/UART/I2C/VI\_BT1120/VI\_BT656  
(1.8V only, some for input only)

VI_BT1120_D0	LVDS_RX_D3N	MIPI_CSI_RX_D3N	VI_CIF_D0 M0	GPIO3_B0 M1	>>	MIPI/LVDS_D3N	7	
VI_BT1120_D1	LVDS_RX_D3P	MIPI_CSI_RX_D3P	VI_CIF_D1 M0	GPIO3_B1 M1	>>	MIPI/LVDS_D3P	7	
VI_BT1120_D2	LVDS_RX_CLKRN	MIPI_CSI_RX_CLKRN	VI_CIF_D2 M0	GPIO3_B2 M1	>>	MIPI/LVDS_CLKIN	7	
VI_BT1120_D3	LVDS_RX_CLKOP	MIPI_CSI_RX_CLKOP	VI_CIF_D3 M0	GPIO3_B3 M1	>>	MIPI/LVDS_CLKIP	7	
VI_BT1120_D4	LVDS_RX_D2N	MIPI_CSI_RX_D2N	VI_CIF_D4 M0	GPIO3_B4 M1	>>	MIPI/LVDS_D2N	7	
VI_BT1120_D5	LVDS_RX_D2P	MIPI_CSI_RX_D2P	VI_CIF_D5 M0	GPIO3_B5 M1	>>	MIPI/LVDS_D2P	7	
VI_BT1120_D6	LVDS_RX_D1N	MIPI_CSI_RX_D1N	VI_CIF_D6 M0	GPIO3_B6 M1	>>	MIPI/LVDS_D1N	7	
VI_BT1120_D7	LVDS_RX_D1P	MIPI_CSI_RX_D1P	VI_CIF_D7 M0	GPIO3_B7 M1	>>	MIPI/LVDS_D1P	7	
VI_BT656_D0 M0	VI_BT1120_D8	LVDS_RX_CLKRN	MIPI_CSI_RX_CLKRN	VI_CIF_D8 M0	GPIO3_C0 M1	>>	MIPI/LVDS_CLKON	7
VI_BT656_D1 M0	VI_BT1120_D9	LVDS_RX_CLKOP	MIPI_CSI_RX_CLKOP	VI_CIF_D9 M0	GPIO3_C1 M1	>>	MIPI/LVDS_CLKOP	7
VI_BT656_CLK M0	VI_BT1120_D10	LVDS_RX_D0N	MIPI_CSI_RX_D0N	VI_CIF_CLKI M0	GPIO3_C2 M1	>>	MIPI/LVDS_D0N	7
		LVDS_RX_D0P	MIPI_CSI_RX_D0P	VI_CIF_HREF M0	GPIO3_C3 M1	>>	MIPI/LVDS_D0P	7
		MIPI_CLKO R49	1 NA 5% 2 R0201	VI_CIF_CLKO M0	GPIO3_C4 M1	>>	MIPI/LVDS_MCLKO	7
		MIPI_CLKI R48	1 NA 5% 2 R0201	VI_CIF_VSYNC M0	GPIO3_C5 M1	>>	MIPI/LVDS_RSTO	7
VI_BT656_D2 M0	VI_BT1120_D11	UART0 RX M2	1204 SCL M2	VI_CIF_D10	GPIO3_C6 M1	>>	MIPI/LVDS_MCLKI	7
VI_BT656_D3 M0	VI_BT1120_D12	UART0 TX M2	1204 SDA M2	VI_CIF_D11	GPIO3_C7 M1	>>	MIPI_I2C4_SCL	7,11
VI_BT656_D4 M0	VI_BT1120_D13	UART0 RTS M2	1203 SCL M2	VI_CIF_D12	GPIO3_D0 M1	>>	MIPI_I2C4_SDA	7,11
VI_BT656_D5 M0	VI_BT1120_D14	UART0 CTS M2	1203 SDA M2	VI_CIF_D13	GPIO3_D1 M1	>>	MIPI_I2C3_SCL	7,11
VI_BT656_D6 M0	VI_BT1120_D15	UART0 RX M2	1203 SDA M2	VI_CIF_D14	GPIO3_D2 M1	>>	MIPI_I2C3_SDA	7,11
VI_BT656_D7 M0	VI_BT1120_D15	PWM1 M2	VI_CIF_D15	GPIO3_D3 M1	>>	MIPI/LVDS_RST1	7	




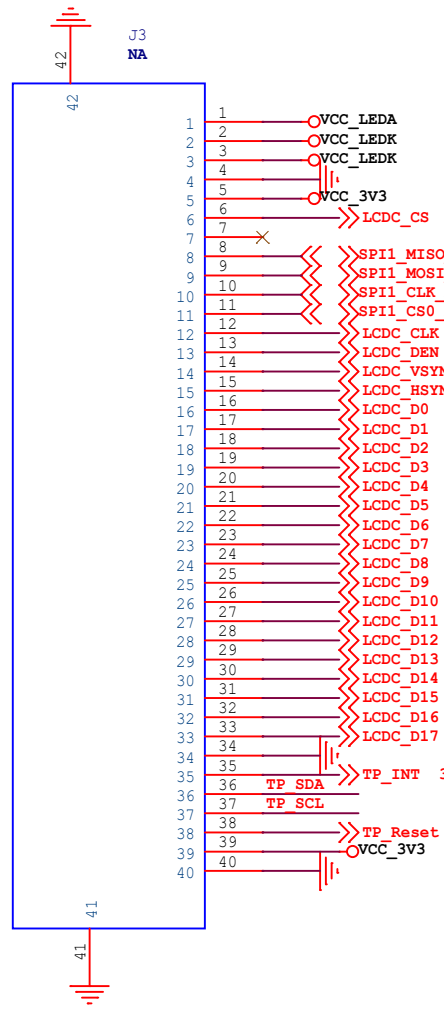
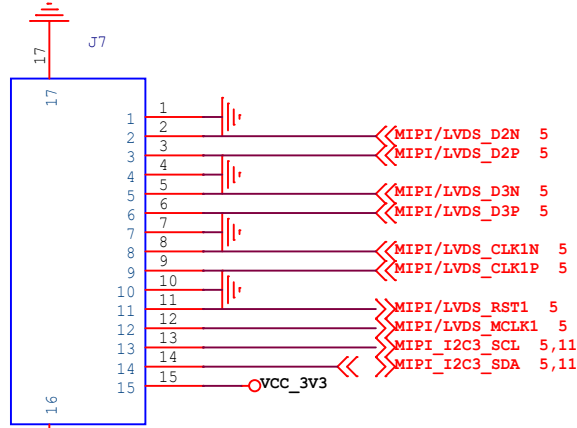
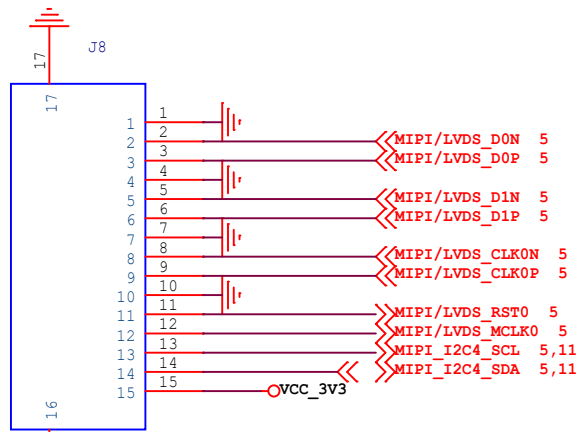
# eMMC

NOTE:  
Refer to the latest AVL for parts selection.

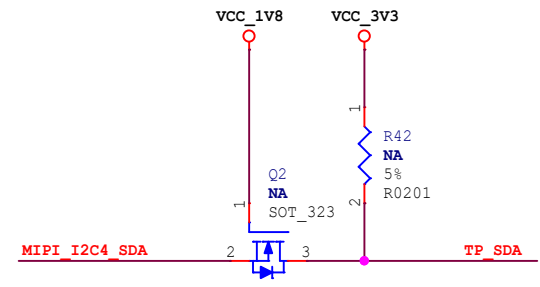
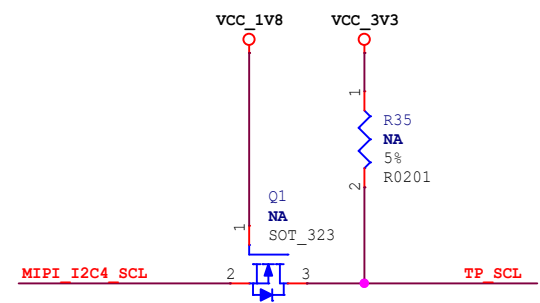
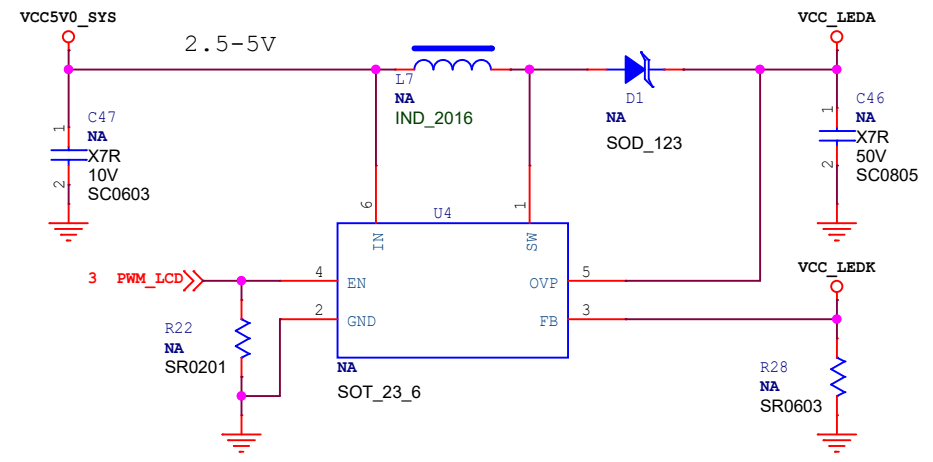



## HINLINK

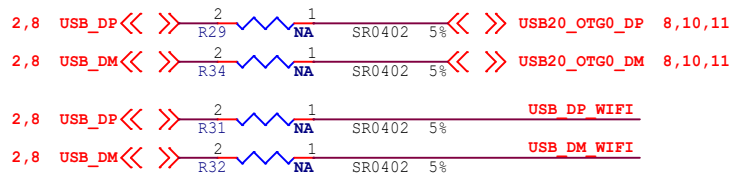
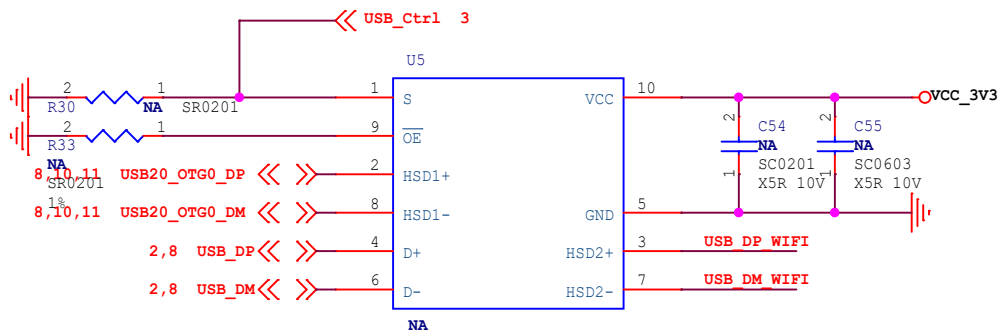
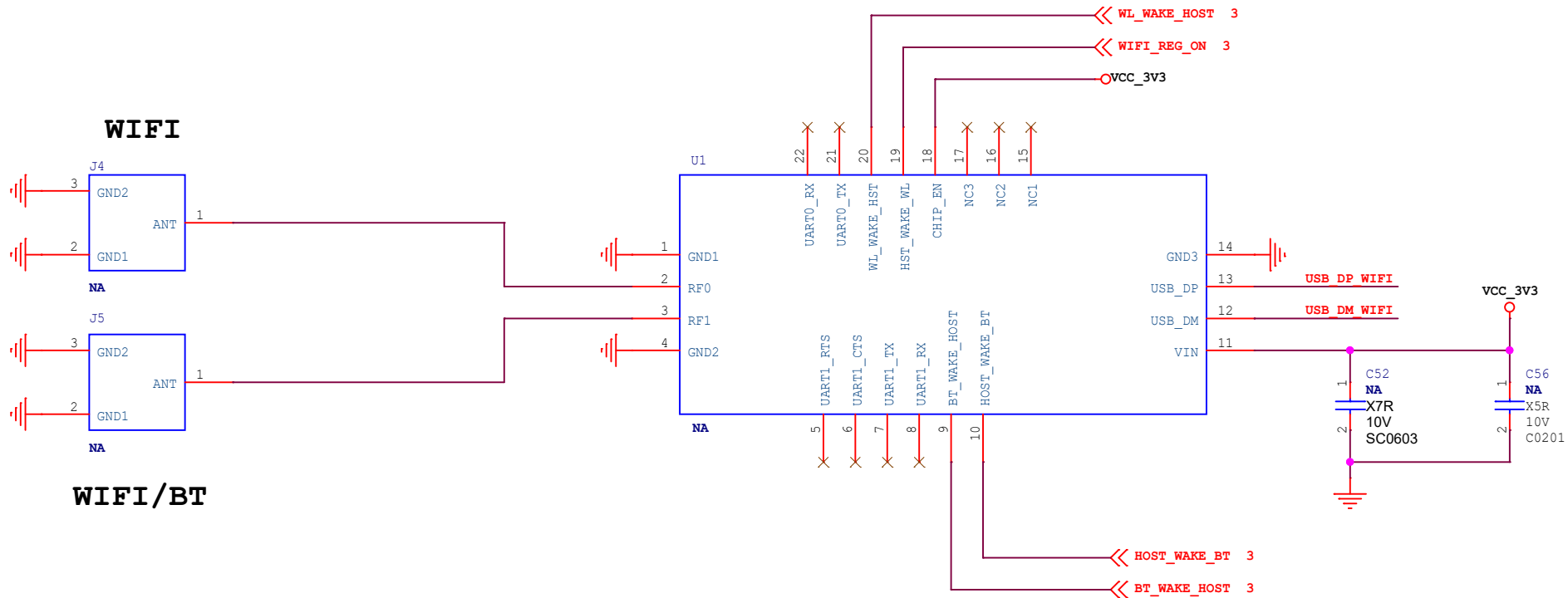
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<b>File:</b>	06.Flash-eMMC Flash	
<b>Date:</b>	Saturday, November 02, 2024	<b>Rev:</b> <Revision>
<b>Designer:</b>	<designer>	<b>Sheet:</b> 6 of 12




第8脚 预留

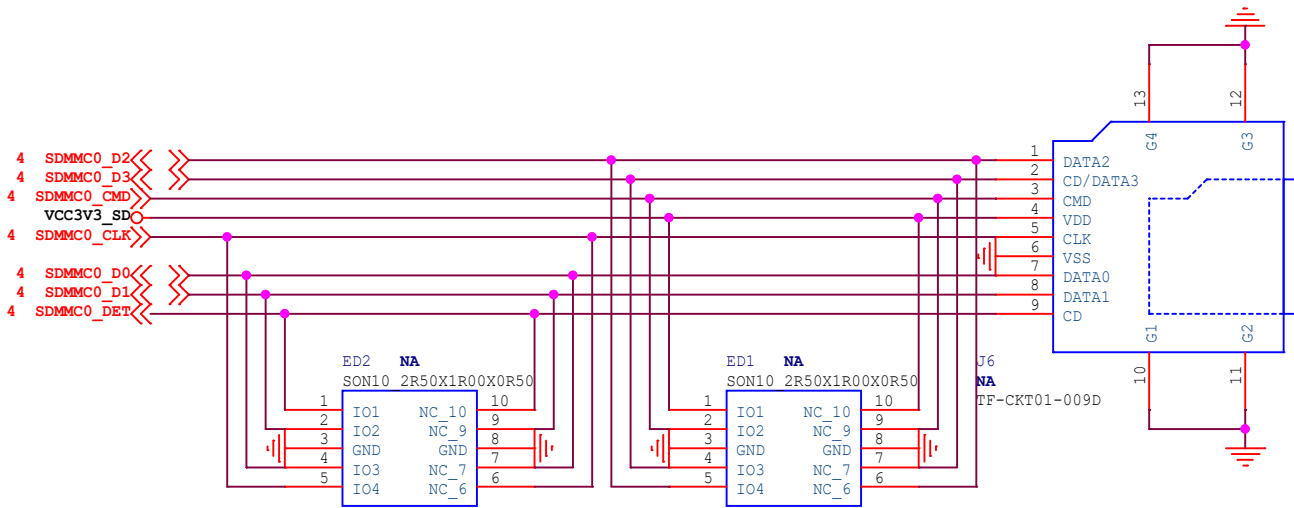


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<b>File:</b>	07.VI-VO	
<b>Date:</b>	Saturday, November 02, 2024	<b>Rev:</b> <Revision>
<b>Designer:</b>	<designer>	<b>Sheet:</b> 7 of 12

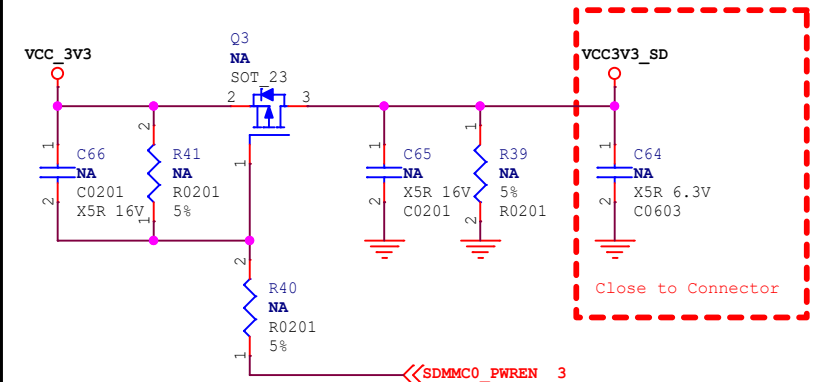


<b>HINLINK</b>		
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<b>File:</b>	<b>08.USB WIFI</b>	
<b>Date:</b>	Saturday, November 02, 2024	<b>Rev:</b> <Revision>
<b>Designer:</b>	<designer>	<b>Sheet:</b> 8 of 12

## Micro-SD Card



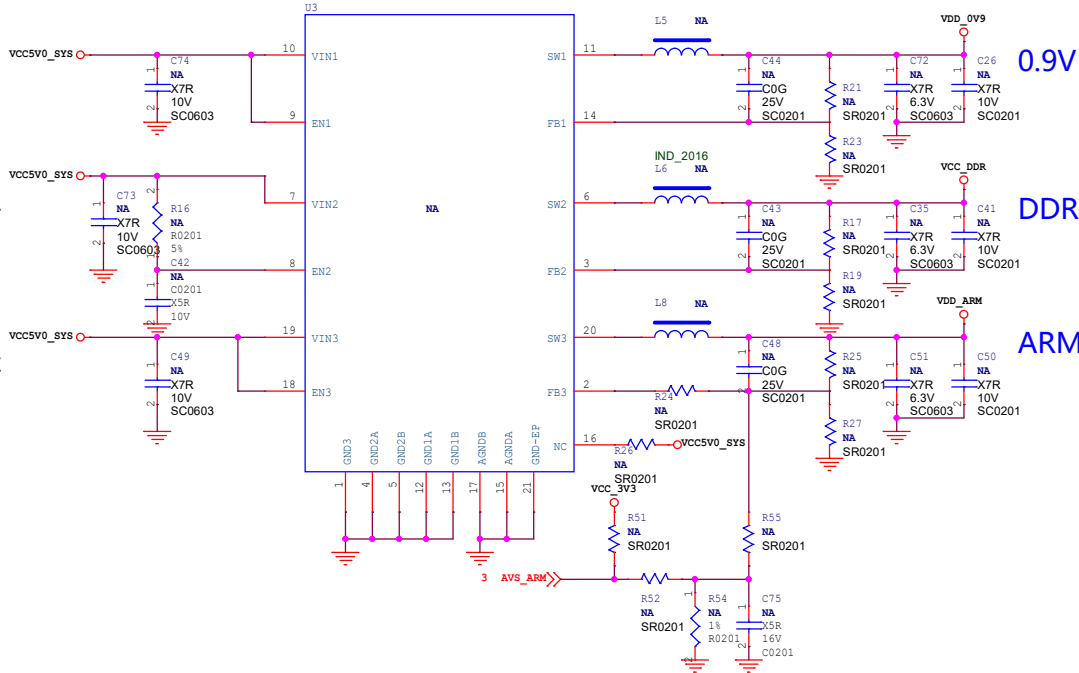
## Card Power



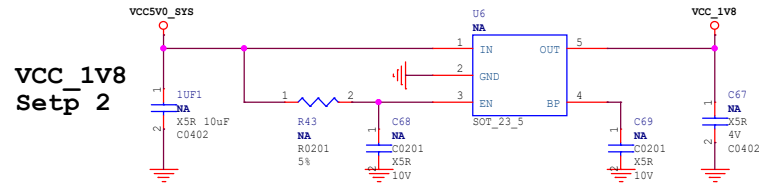
SDMMC0\_PWREN=L VCC3V3\_SD=3.3V(Default)  
 SDMMC0\_PWREN=H VCC3V3\_SD=0V

<b>HINLINK</b>		
<b>Project:</b>	SoloLinker-A	
<b>File:</b>	09.SD Card	
<b>Date:</b>	Saturday, November 02, 2024	<b>Rev:</b> <Revision>
<b>Designer:</b>	<designer>	<b>Sheet:</b> 9 of 12

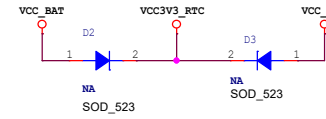
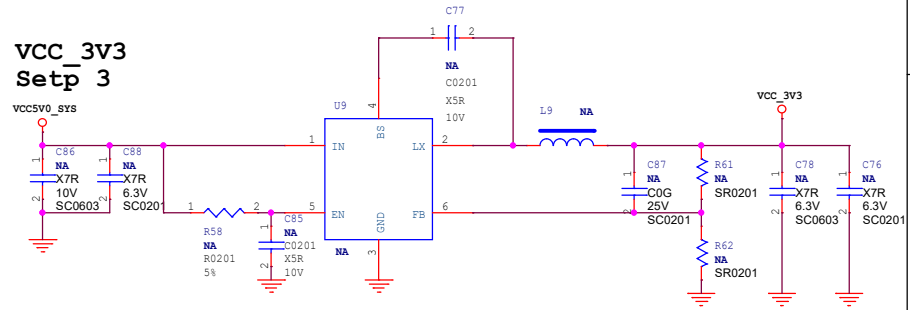
**VDD\_0V9  
Setp 1**



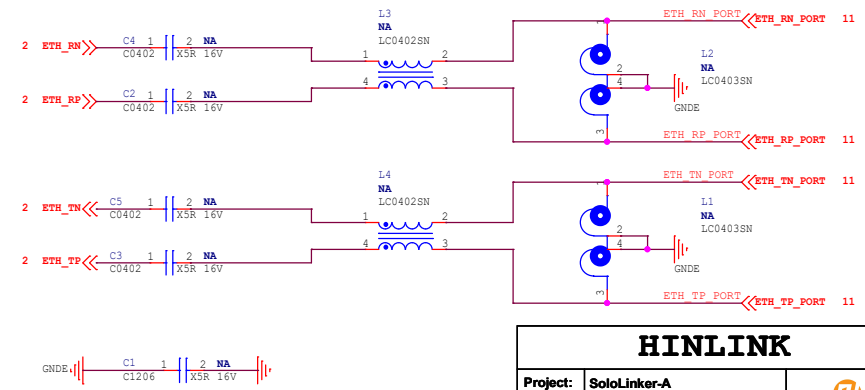
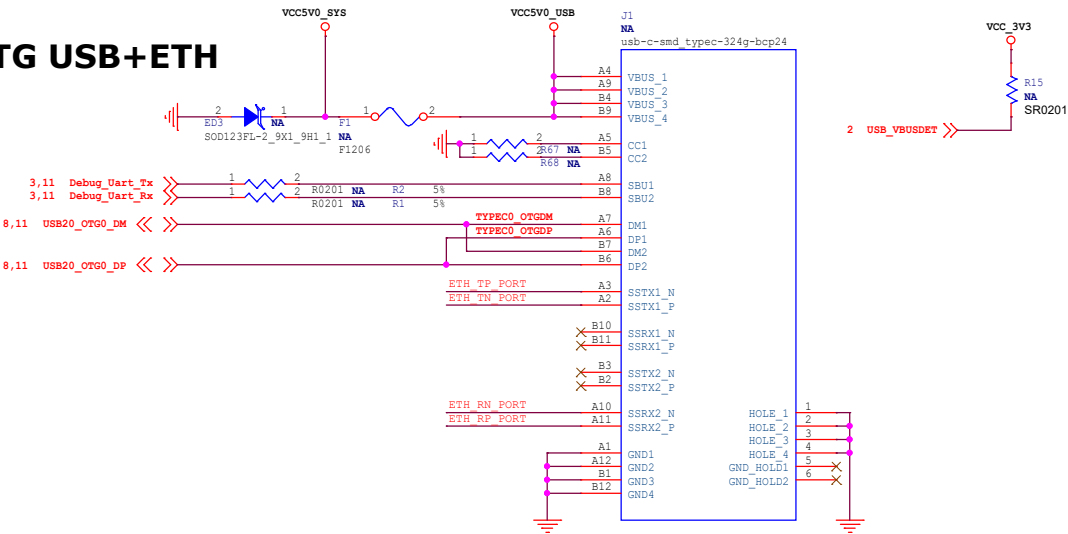
**VCC\_DDR  
Setp 2**



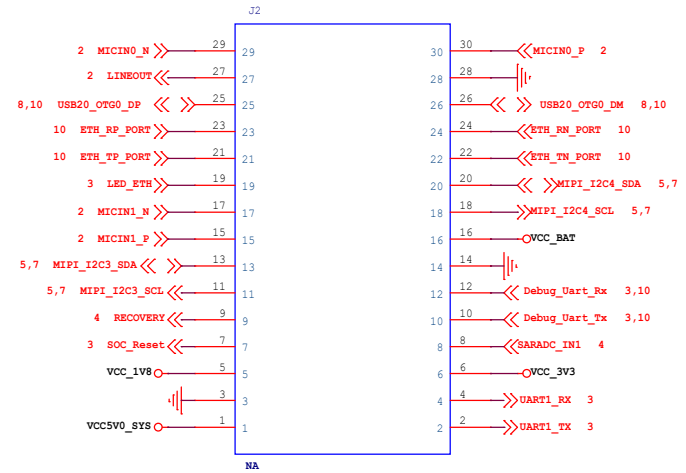
**VCC\_3V3  
Setp 3**




**OTG USB+ETH**



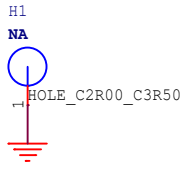
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<b>Date:</b>	Saturday, November 02, 2024		
<b>Designer:</b>	<designer>		
<b>Rev:</b>	<Revision>	<b>Sheet:</b>	10 of 12



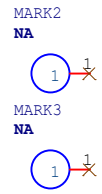
# HINLINK

Project:	SoloLinker-A	 HINLINK
File:	11.HC1106_2MM54	
Date:	Saturday, November 02, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 11 of 12


**HOLE**



**MARK**



**HINLINK**

<b>HINLINK</b>			
<b>Project:</b>	SoloLinker-A	 <b>HINLINK</b>	
<b>File:</b>	12.Mark/Hole		
<b>Date:</b>	Saturday, November 02, 2024	<b>Rev:</b>	<Revision>
<b>Designer:</b>	<designer>	<b>Sheet:</b>	12 of 12