Reference Schematics For RK3528

RK3528_BOX_REF_SCH_V10

Main Functions Introduction

1) Power: DiscretePower:BUCK+LDO or PMIC RK805-6
2) RAM: DDR3 4x16bit
DDR4 2x16Bit
DDR4 4x16Bit
LPDDR3 1x32bit
LPDDR4/LPDDR4X 1x32bit
3) ROM: eMMC5.1 or FSPI Flash
4) Support: Micro SD Card3.0
5) Support: 1 x USB3.0 OTG + 1 x USB2.0 HOST
6) Support: 1 x HDMI2.0 TX
7) Support: 1 x AV OUT
8) Support: SDIO WiFi5 + UART/PCM BT
PCIE WIFI5 + UART/PCM BT
9) Support: 1 x Ethernet(Embed PHY) + 1x Ethernet(RGMII or RMII)
10) Support: Optical S/PDIF TX
11) Support: IR Receiver
12) Support: Audio-MicArray 2xI2S-DMIC or 4xPDM-DMIC
13) Support: RECOVER/RESET/SARADC_BOOT_KEY,HW_ID
14) Support: 1 x PCIE2.0 Slot
15) Support: Debug UART

HINLINK

Project:	**RK3528_HT2**	HINLINK	
File:	**00.Cover Page**		
Date:	Friday, December 08, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	1 of 23

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Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

HINLINK

Project:	**RK3528_HT2**	HINLINK	
File:	**01.Index and Notes**		
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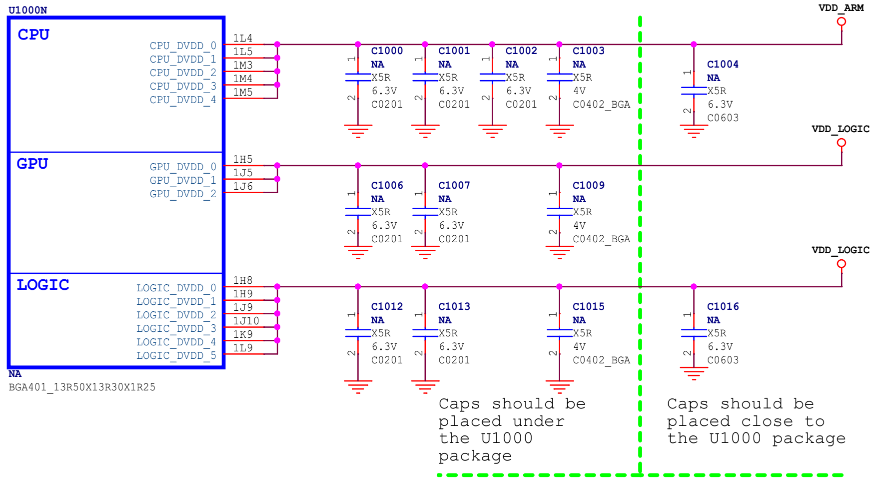
RK3528_N(POWER)



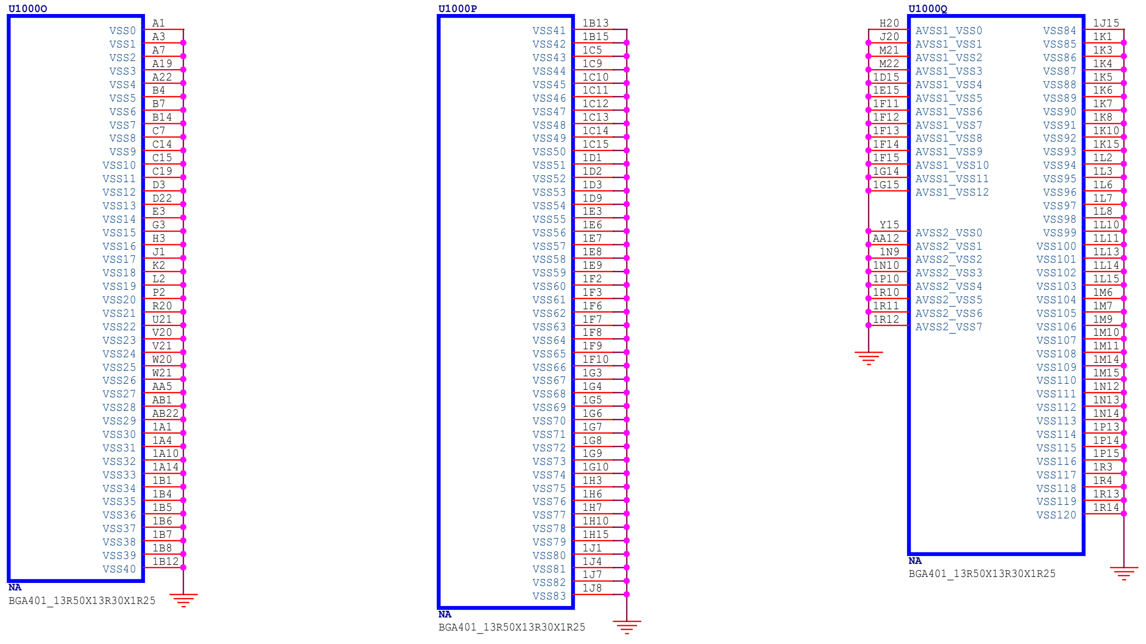
Caps should be placed under the U1000 package

Caps should be placed close to the U1000 package

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_O/P/Q(GND)



HINLINK

Project:	RK3528_HT2		
File:	02.RK3528 Power/GND		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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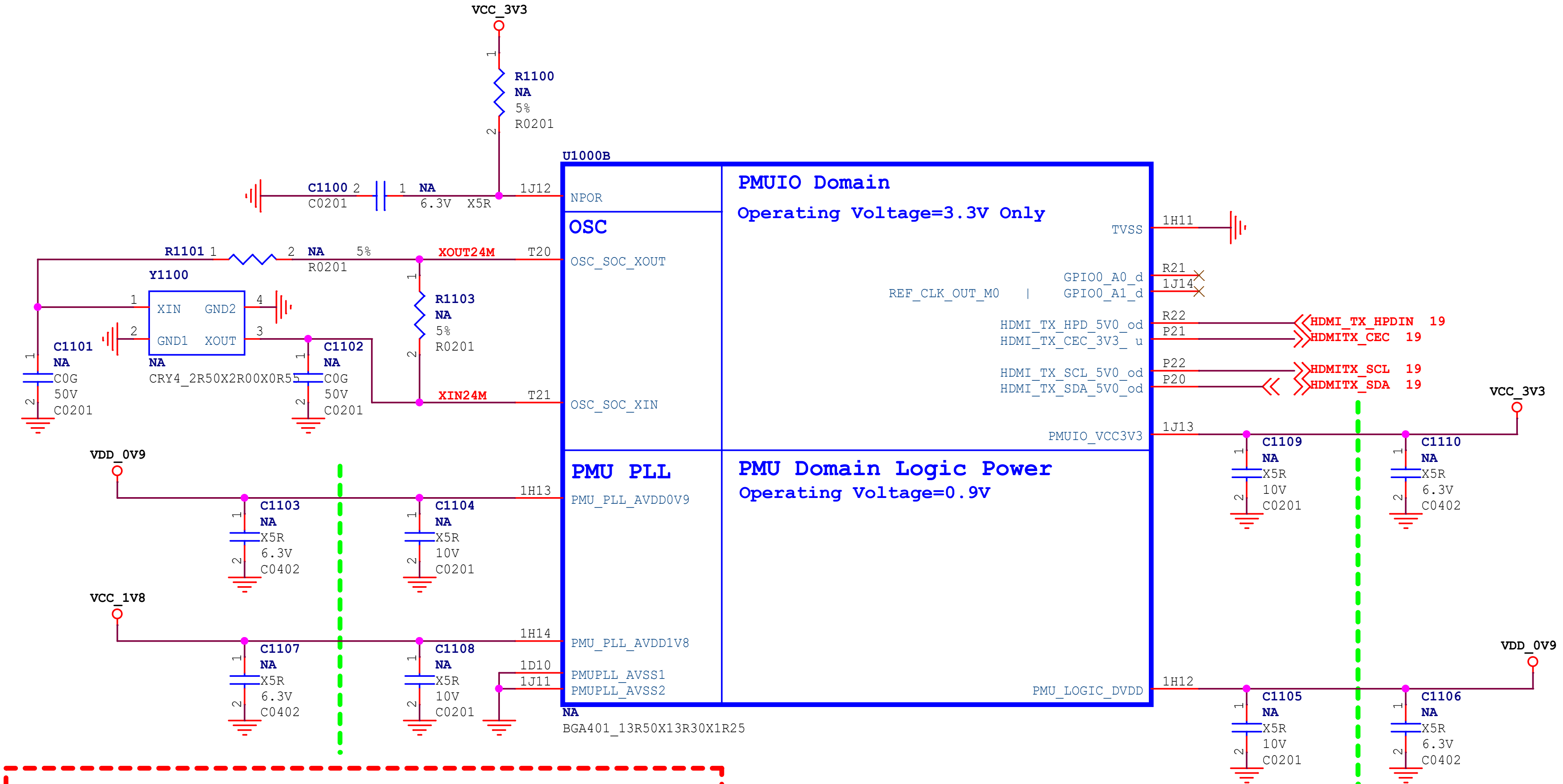
RK3528_B(OSC/PLL/PMUIO Domain)



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

HINLINK

Project:	**RK3528_HT2**	HINLINK	
File:	**03.RK3528 OSC/PLL/PMUIO**		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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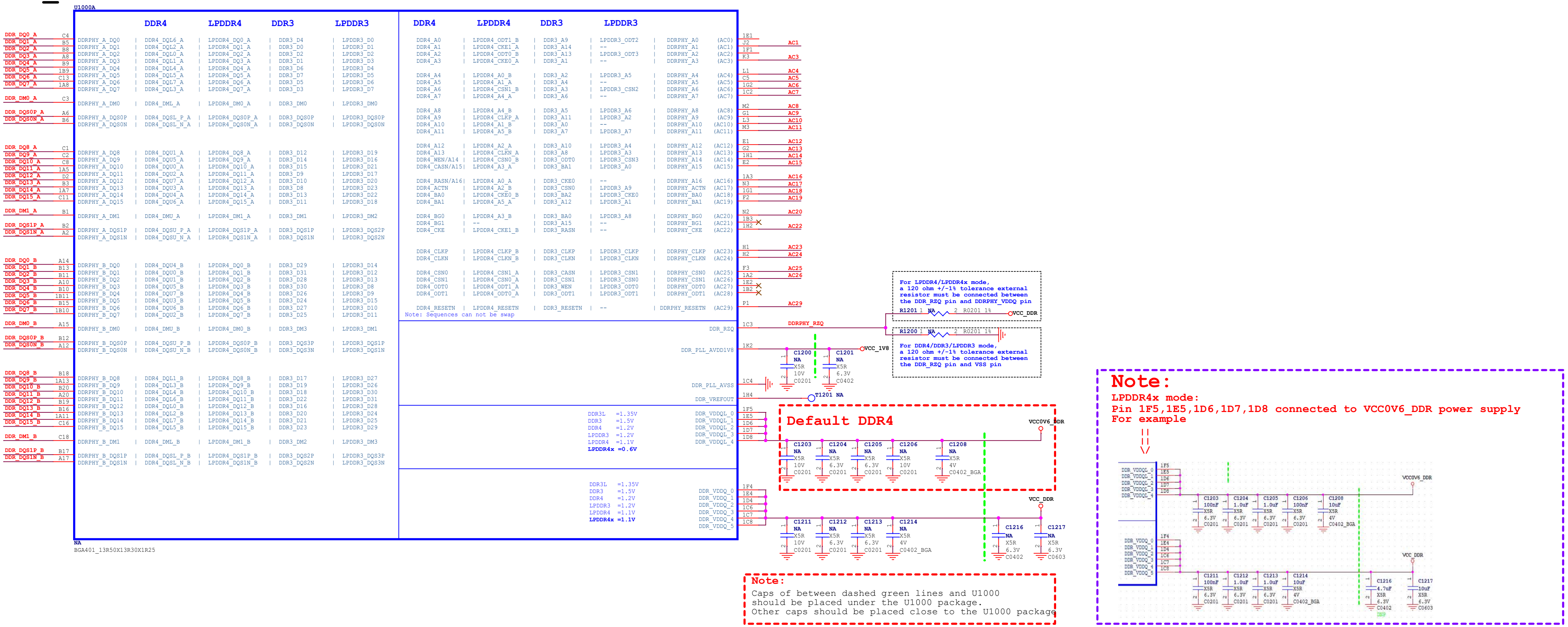
RK3528_A(DDR PHY)



Note: Sequences can not be swap

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

Default DDR4

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

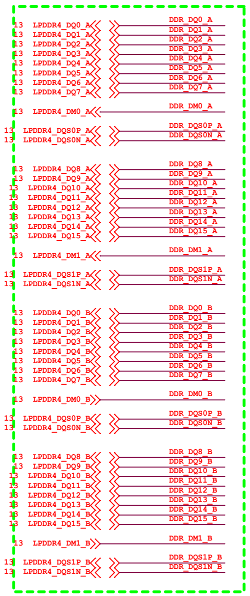
Note:

LPDDR4x mode:

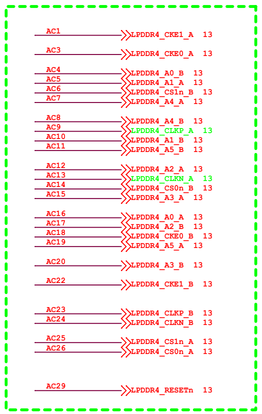
Pin 1F5,1E5,1D6,1D7,1D8 connected to VCC0V6_DDR power supply

For example

LPDDR4/4x DQ



LPDDR4/4x AC



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Project:	RK3528_HT2		
File:	04.RK3528 DDR Controller		
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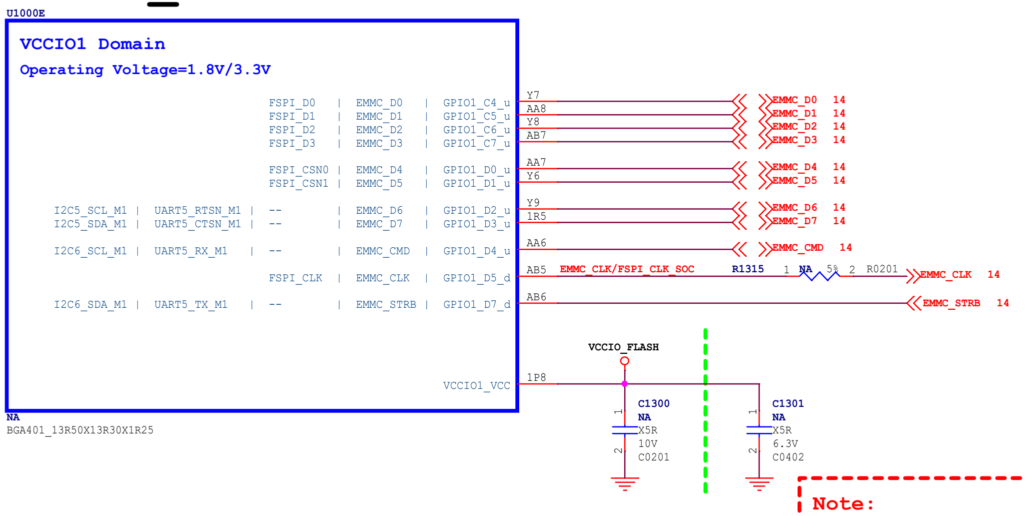
RK3528_E(VCCIO1 Domain)



FSPI(Flexible Serial Peripheral Interface) is only used to connect SPI Flash/Memory devices.
Do not use for connecting to other SPI devices

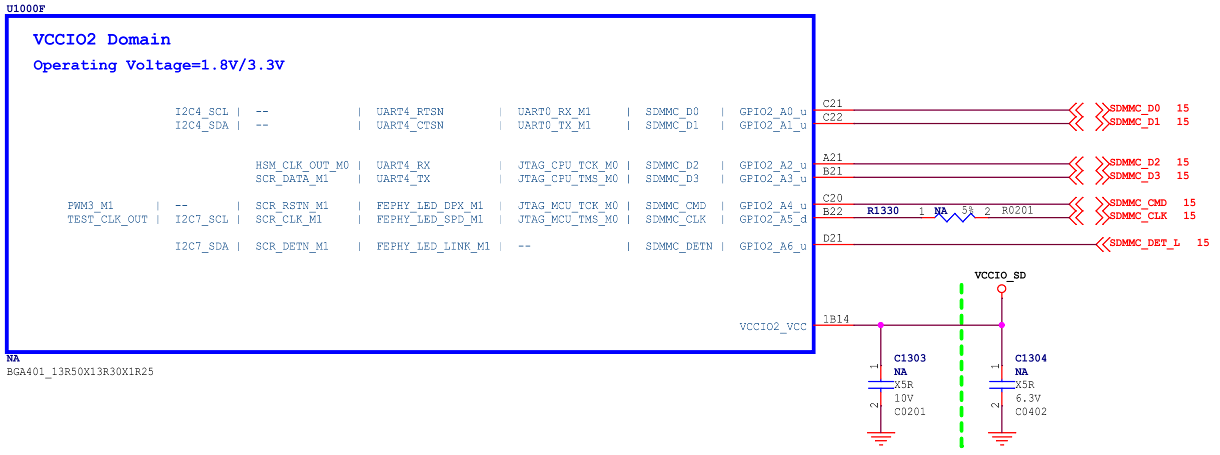
Default
DiscretePower solution, power by VCC_1V8

PMIC solution, power by VCC1V8_EMMC,only 1.8V

Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_F(VCCIO2 Domain)



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

HINLINK			
Project:	RK3528_HT2		
File:	05.RK3528 FLASH/SD Controller		
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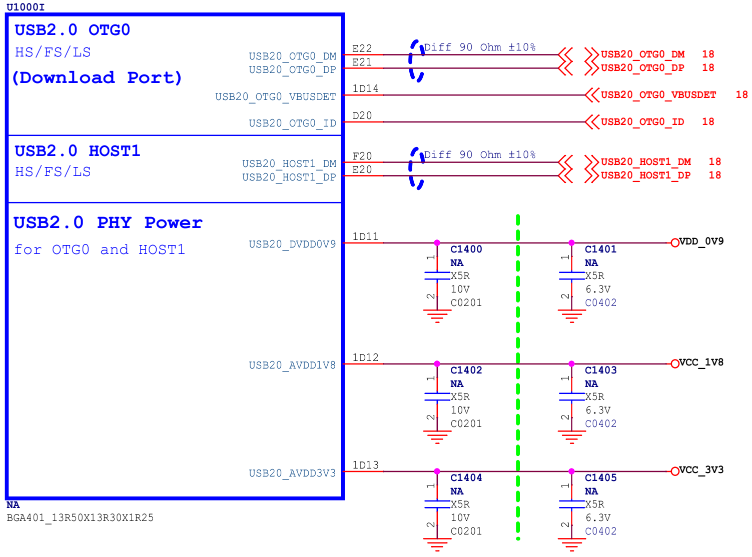
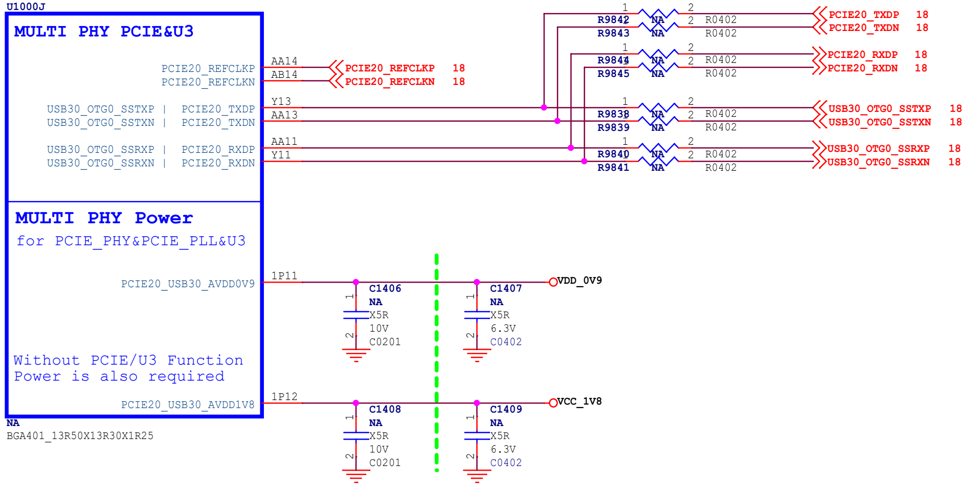
RK3528_I(USB2.0 OTG/HOST)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_J(PCIE2.0/U3 PHY)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

HINLINK

Project:	RK3528_HT2		
File:	06.RK3528 USB/PCIE Controller		
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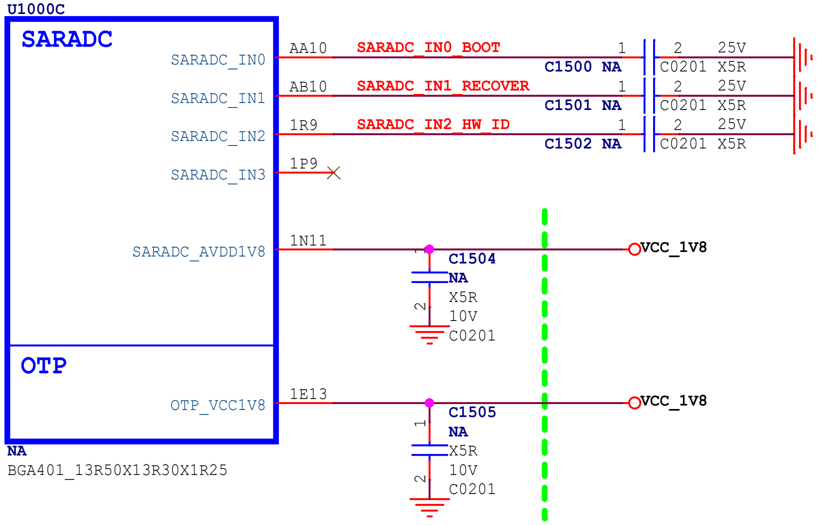
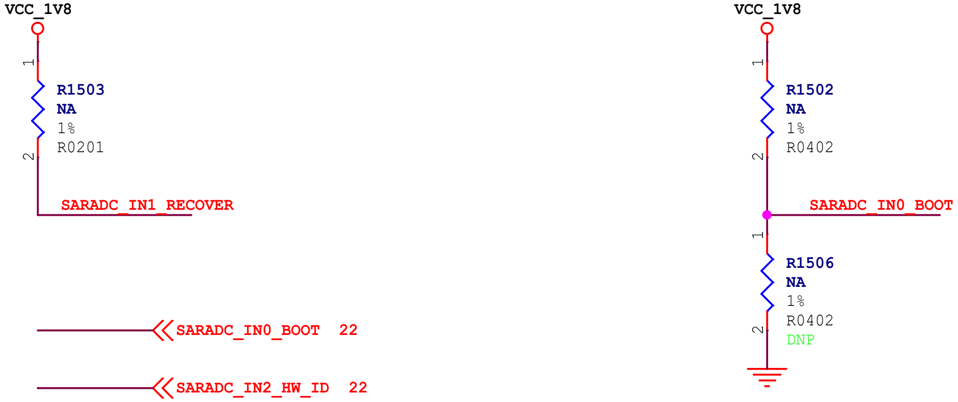
RK3528_C(Saradc/OTP)



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



TABLE

Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	12K	114	
LEVEL3	100K	27K	228	FSPI--USB
LEVEL4	100K	51K	342	
LEVEL5	100K	82K	456	
LEVEL6	100K	120K	570	EMMC--USB
LEVEL7	100K	200K	683	EMMC--SD Card--USB
LEVEL8	100K	330K	796	SD Card--USB
LEVEL9	100K	820K	910	
LEVEL10	100K	DNP	1023	FSPI--EMMC--SD Card--USB

HINLINK

Project:	RK3528_HT2		
File:	07.RK3528 SARADC/OTP		
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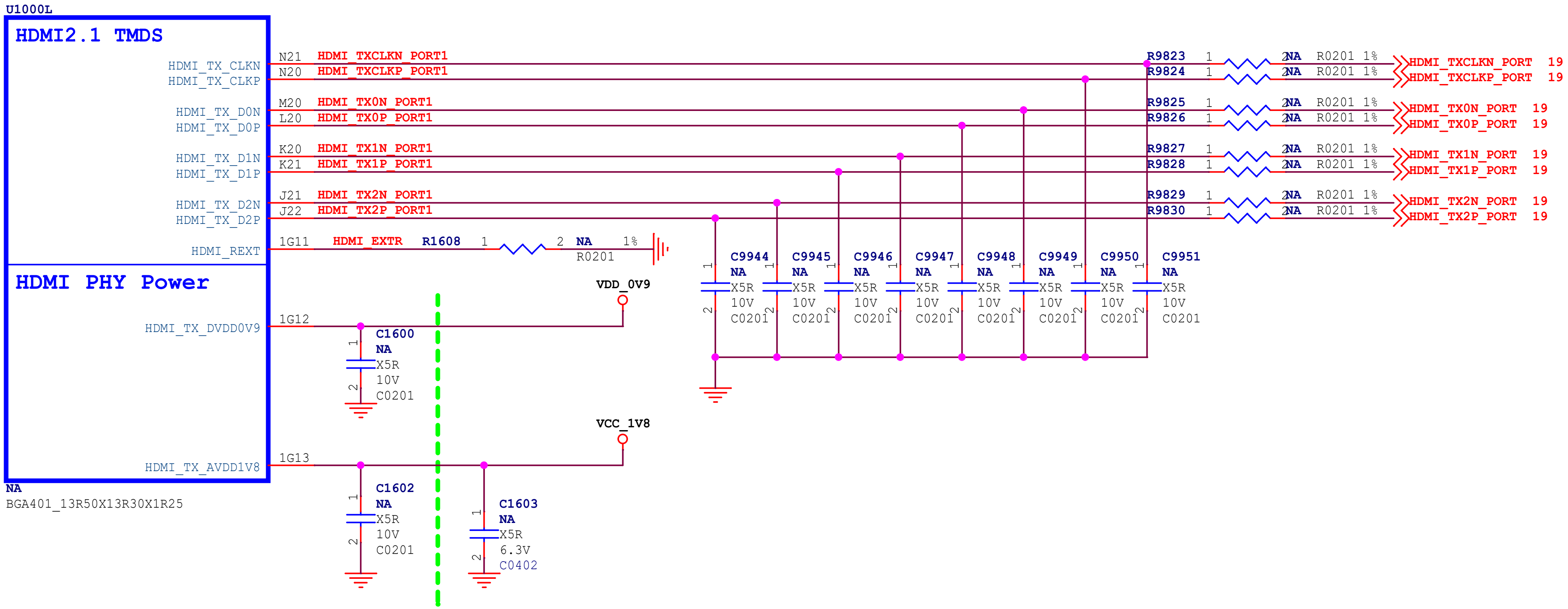
RK3528_L(HDMI PHY)



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

HINLINK

Project:	RK3528_HT2		
File:	08.RK3528 HDMI Interface		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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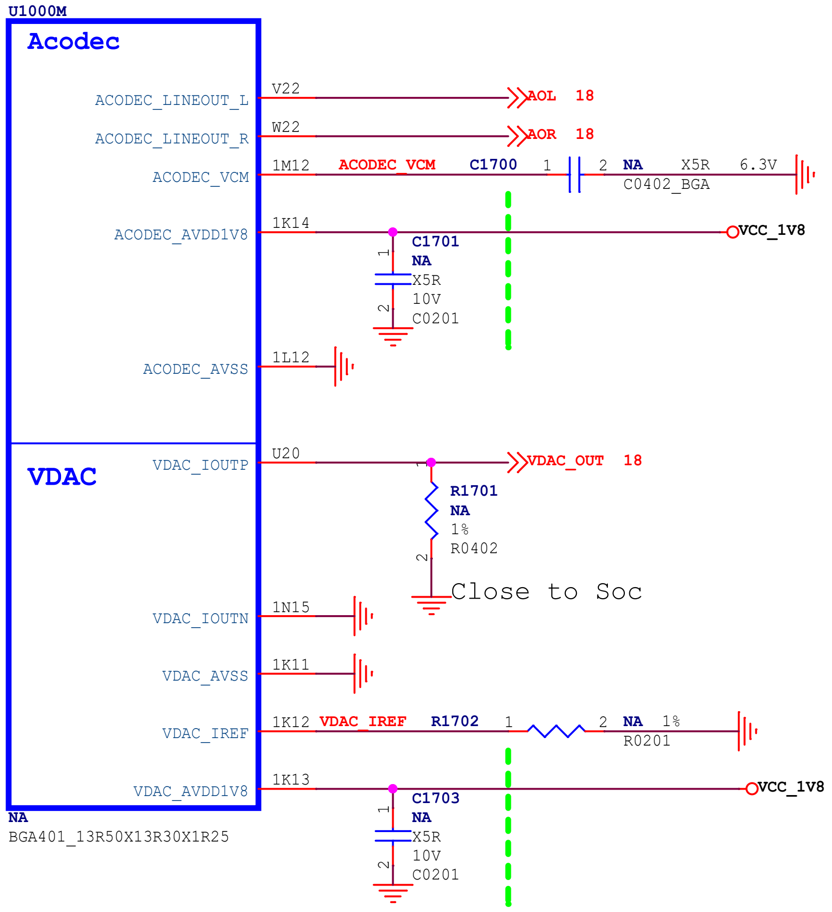
RK3528_M(Acodec/VDAC)



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

HINLINK

Project:	**RK3528_HT2**		
File:	**09.RK3528 AV OUT**		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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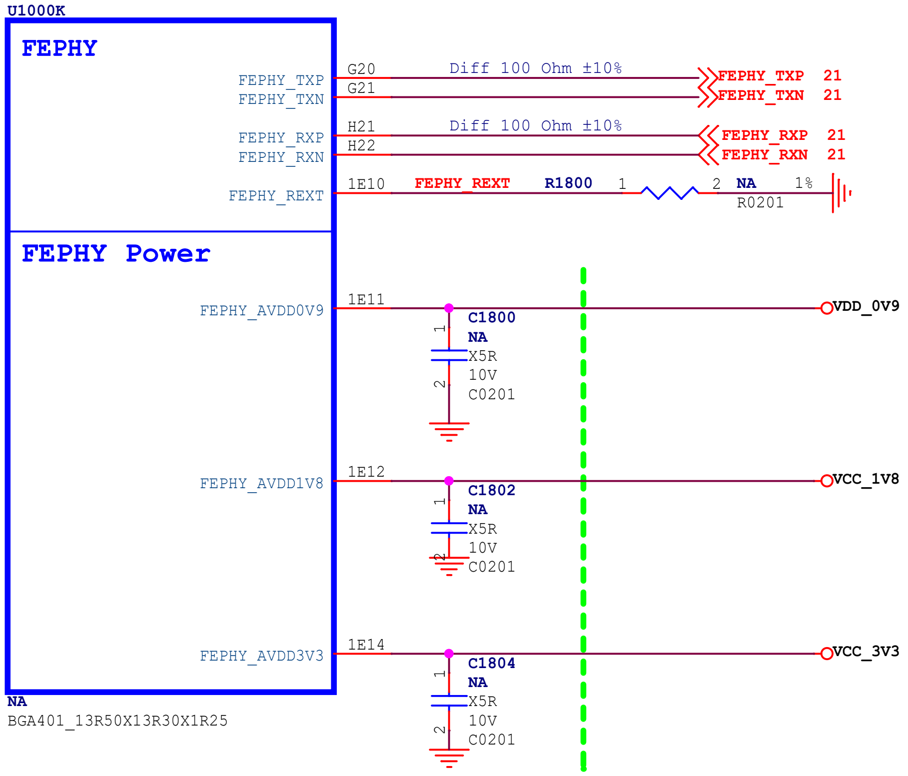
RK3528_K(Embed FEPHY)



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

HINLINK			
Project:	**RK3528_HT2**		
File:	**10.RK3528 Embed FEPHY**		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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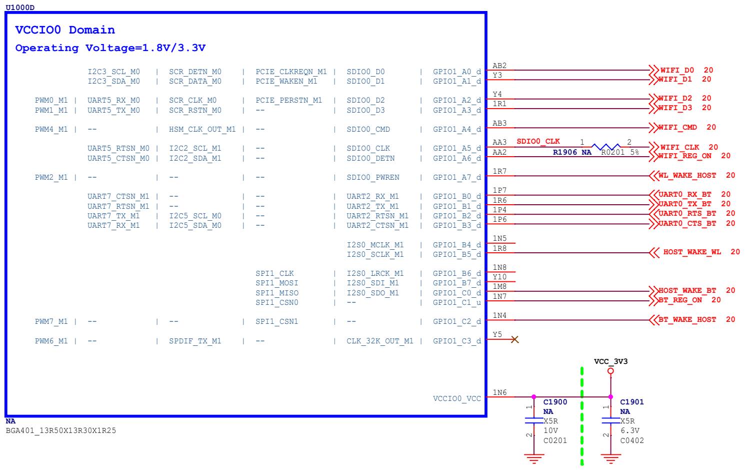
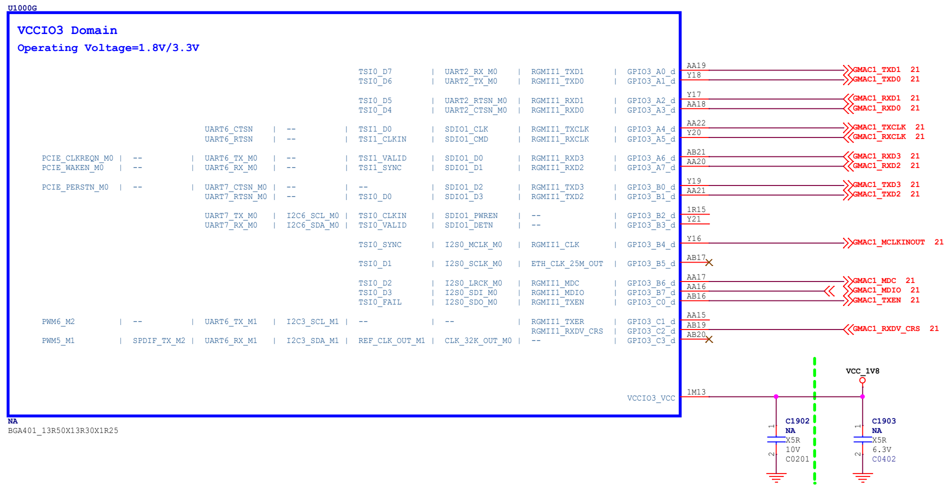
RK3528_D(VCCIO0 Domain)



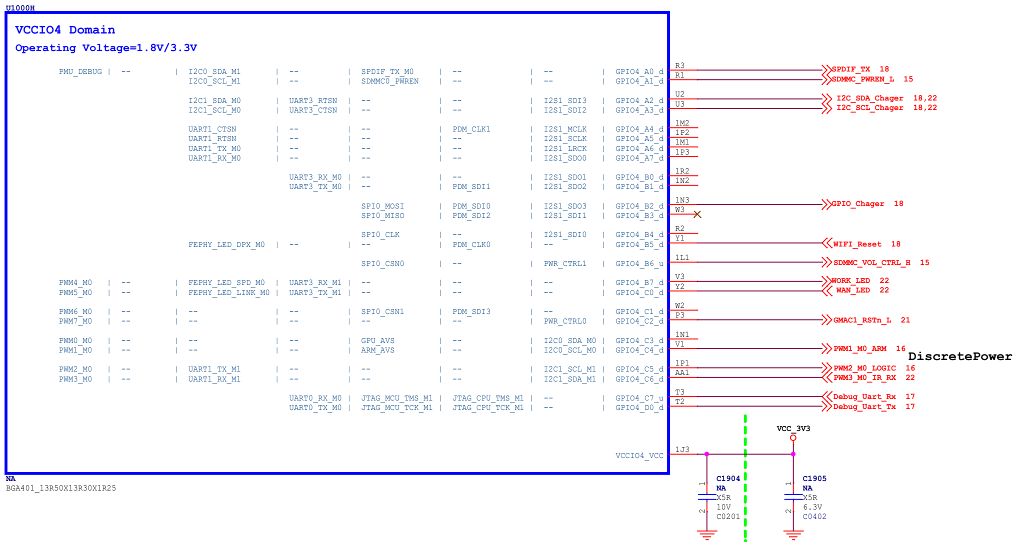
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_G(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_H(VCCIO4 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

HINLINK

Project:	RK3528_HT2		
File:	11.RK3528_1.8V/3.3V GPIO		
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eMMC

HINLINK

Project:	**RK3528_HT2**		
File:	**13.Flash-eMMC**		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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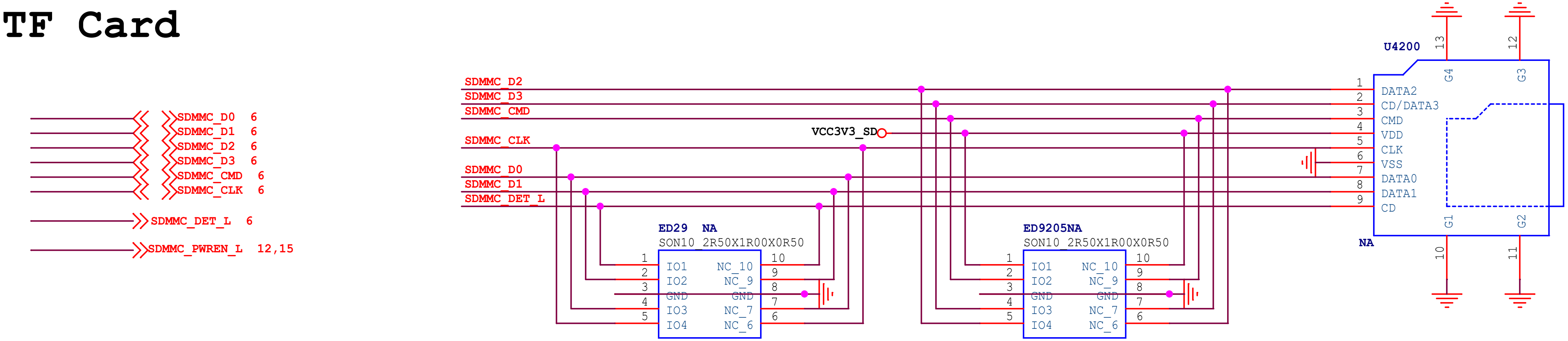
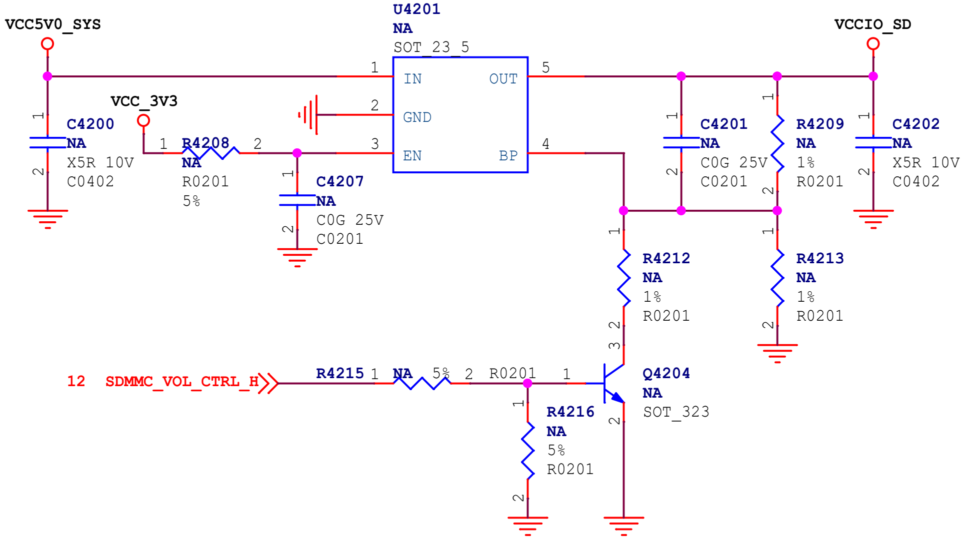
TF Card

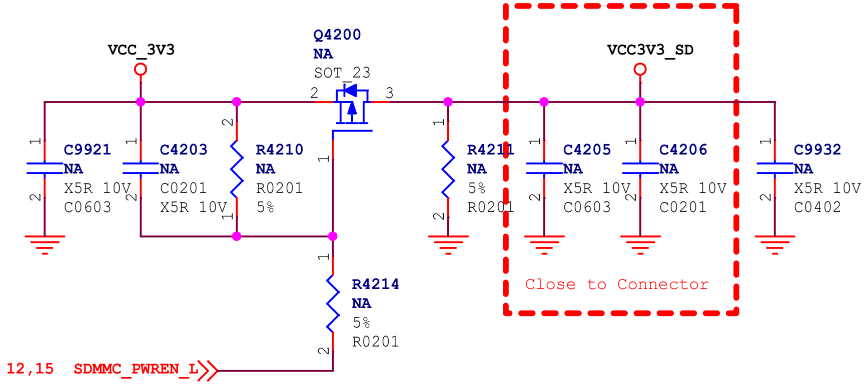


VCCIO_SD



SDIO2.0 SDMMC0_VOL_CTRL=H VCCIO_SD=3.34V(Default)
SDIO3.0 SDMMC0_VOL_CTRL=L VCCIO_SD=1.816V

VCC3V3_SD



SDMMC_PWREN=L VCC_SD=3.3V(Default)
SDMMC_PWREN=H VCC_SD=0V

HINLINK

Project:	RK3528_HT2		
File:	14.Flash-Micro-SD Card		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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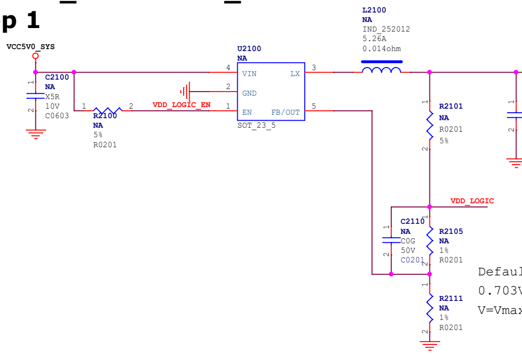
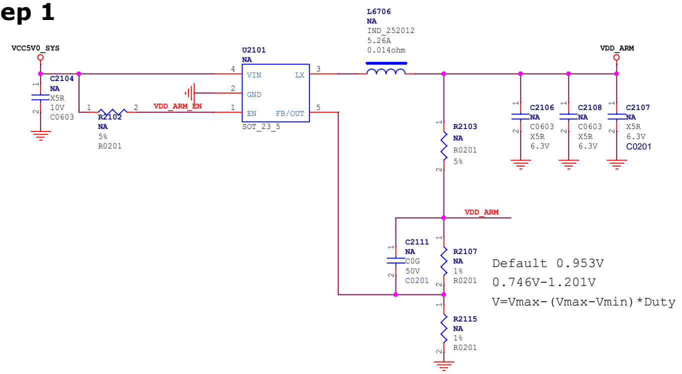
VCC5V0_SYS-->VDD_LOGIC
Step 1



Default 0.901V
0.703V-1.006V
V=Vmax-(Vmax-Vmin)*Duty

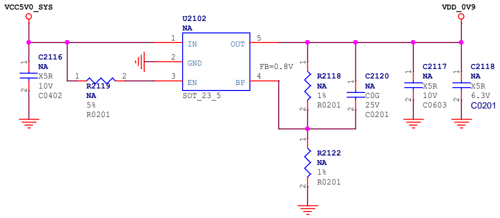
VCC5V0_SYS-->VDD_ARM
Step 1



Default 0.953V
0.746V-1.201V
V=Vmax-(Vmax-Vmin)*Duty

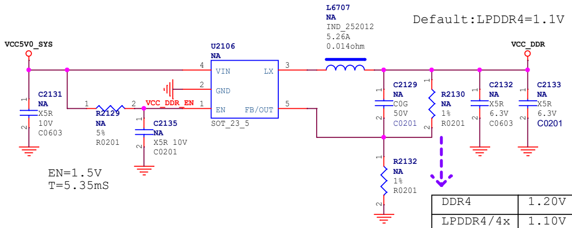
VCC5V0_SYS-->VDD_0V9
Step 1

Note:
When LAYOUT, a star must be used,
Branch to each load



VCC5V0_SYS-->VCC_DDR
Step 2

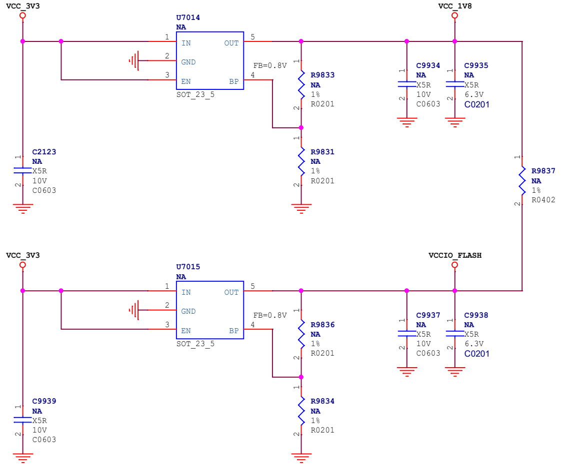
Default:LPDDR4=1.1V



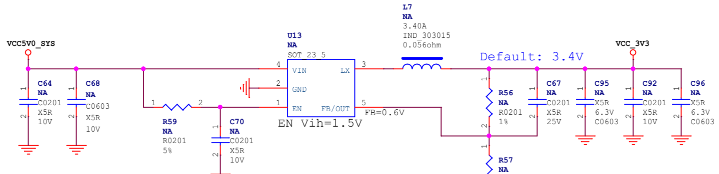
EN=1.5V
T=5.35mS

DDR4	1.20V	100K	1%
LPDDR4/4x	1.10V	84.5K	1%
DDR3	1.5V	150K	1%
DDR3L	1.35V	127K	1%
LPDDR3	1.25V	110K	1%

VCC_3V3->VCC_1V8(LDO)
Step 2



VCC5V0_SYS-->VCC_3V3
Step 2



Default: 3.4V

EN Vih=1.5V

IF R=12k,C=100nF, RC delay:2.2ms
default R=12k,, delay time:2.2ms
1.8V start time:2ms
total delay time=4.2ms

HINLINK

Project:	RK3528_HT2	HINLINK	
File:	15.Power-DiscretePower		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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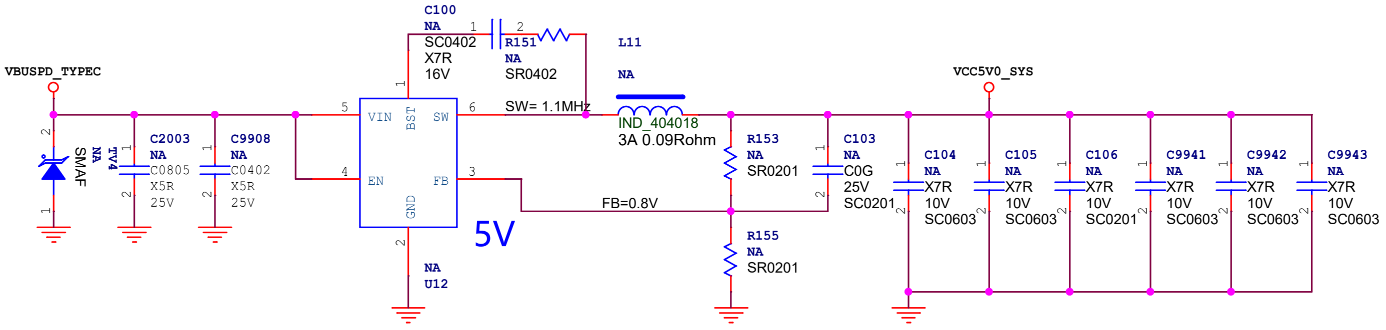
5V_SYS



USB+Debug

HINLINK			
Project:	**RK3528_HT2**		
File:	**16.Power-DCIN**		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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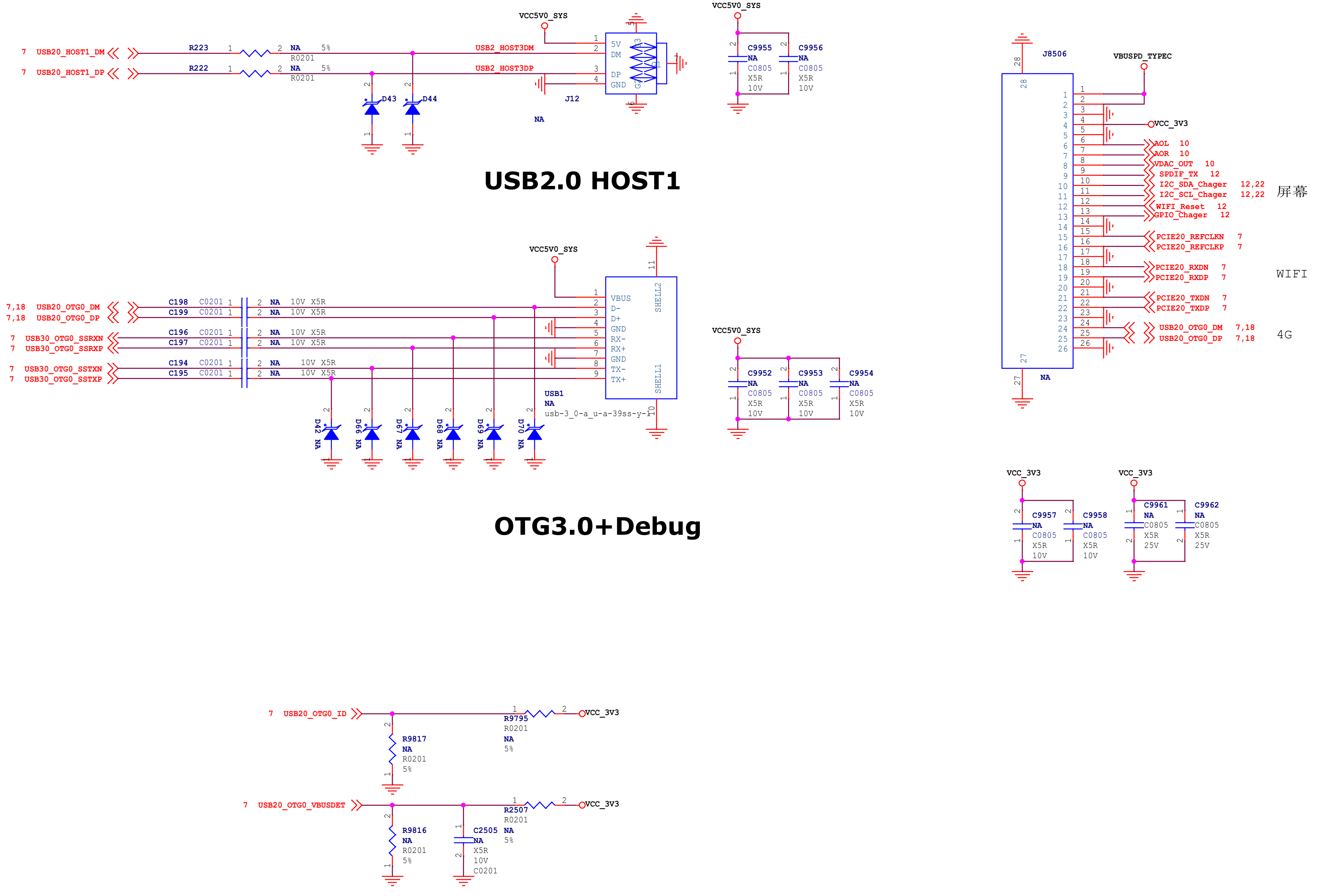

HINLINK

Project:	RK3528_HT2		
File:	17.USB3.0+2.0 Port		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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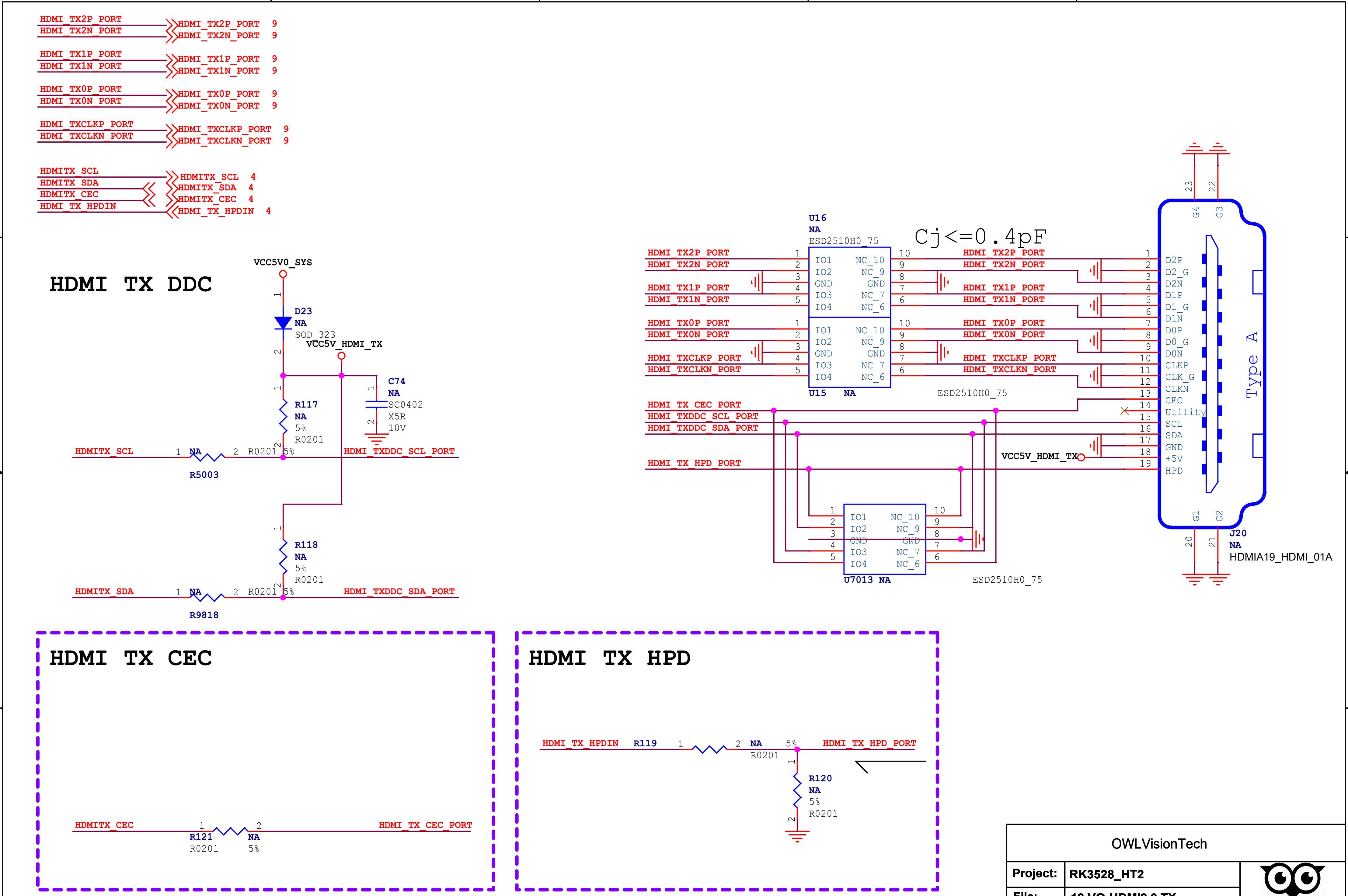

OWLVisionTech

Project:	**RK3528_HT2**		
File:	**18.VO-HDMI2.0 TX**		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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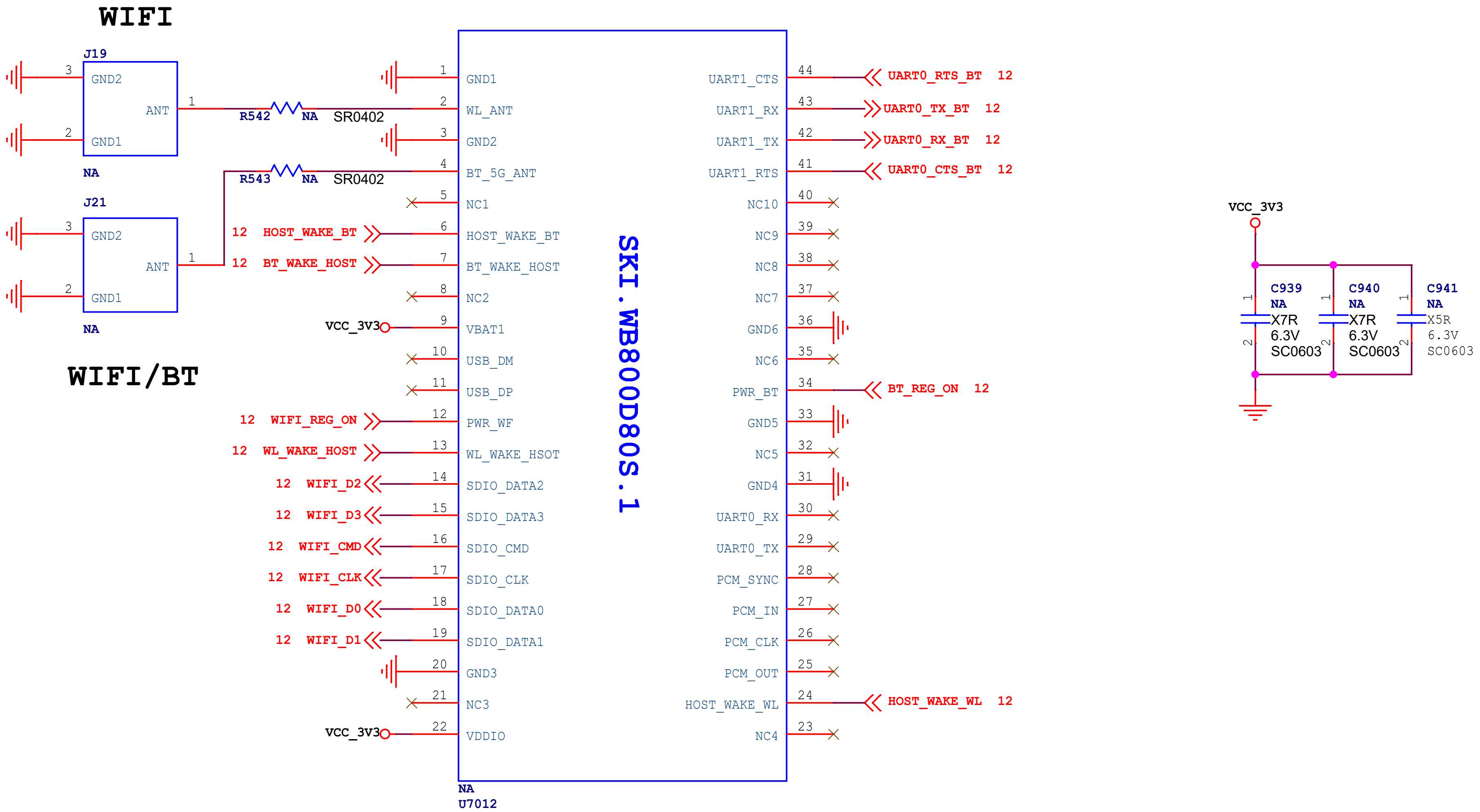
OWLVisionTech

Rockchip Confidential



HINLINK

Project:	**RK3528_HT2**	HINLINK	
File:	**19.WIFI**		
Date:	Monday, January 29, 2024	Rev:	<Revision>
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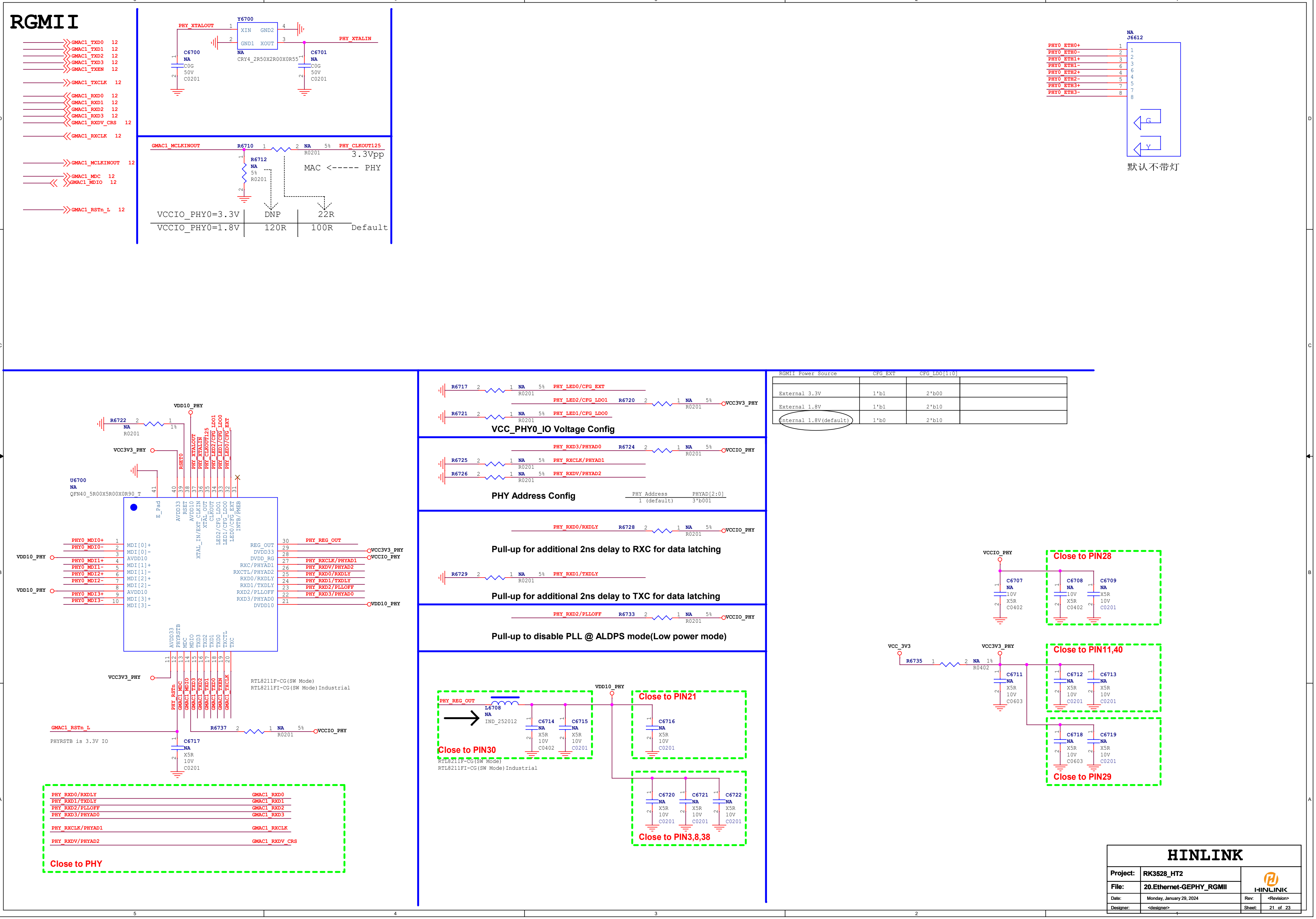
RGMII



RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	

HINLINK

Project:	RK3528_HT2		
File:	20.Ethernet-GEPHY_RGMII		
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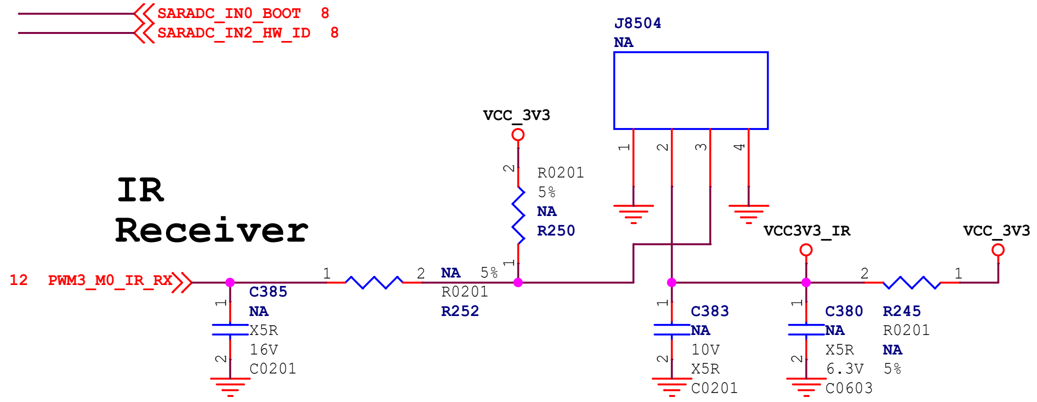
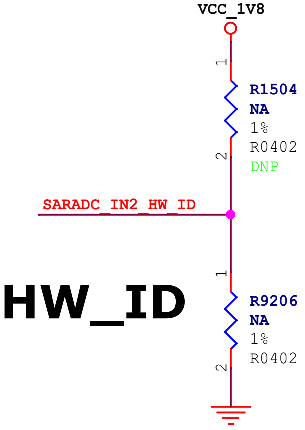
KEY

IR Receiver



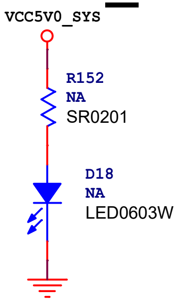
HW_ID



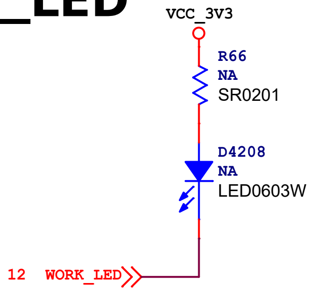
V1.0 **TABLE**

SARADC_IN2	Rup	Rdown	ADC
HW_ID0	DNP	100K	0
HW_ID1	100K	12K	114
HW_ID2	100K	27K	228
HW_ID3	100K	51K	342
HW_ID4	100K	82K	456
HW_ID5	100K	120K	570
HW_ID6	100K	200K	683
HW_ID7	100K	330K	796
HW_ID8	100K	820K	910
HW_ID9	100K	DNP	1023

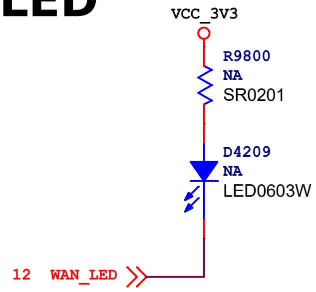
POWER_LED



WORK_LED



WAN_LED



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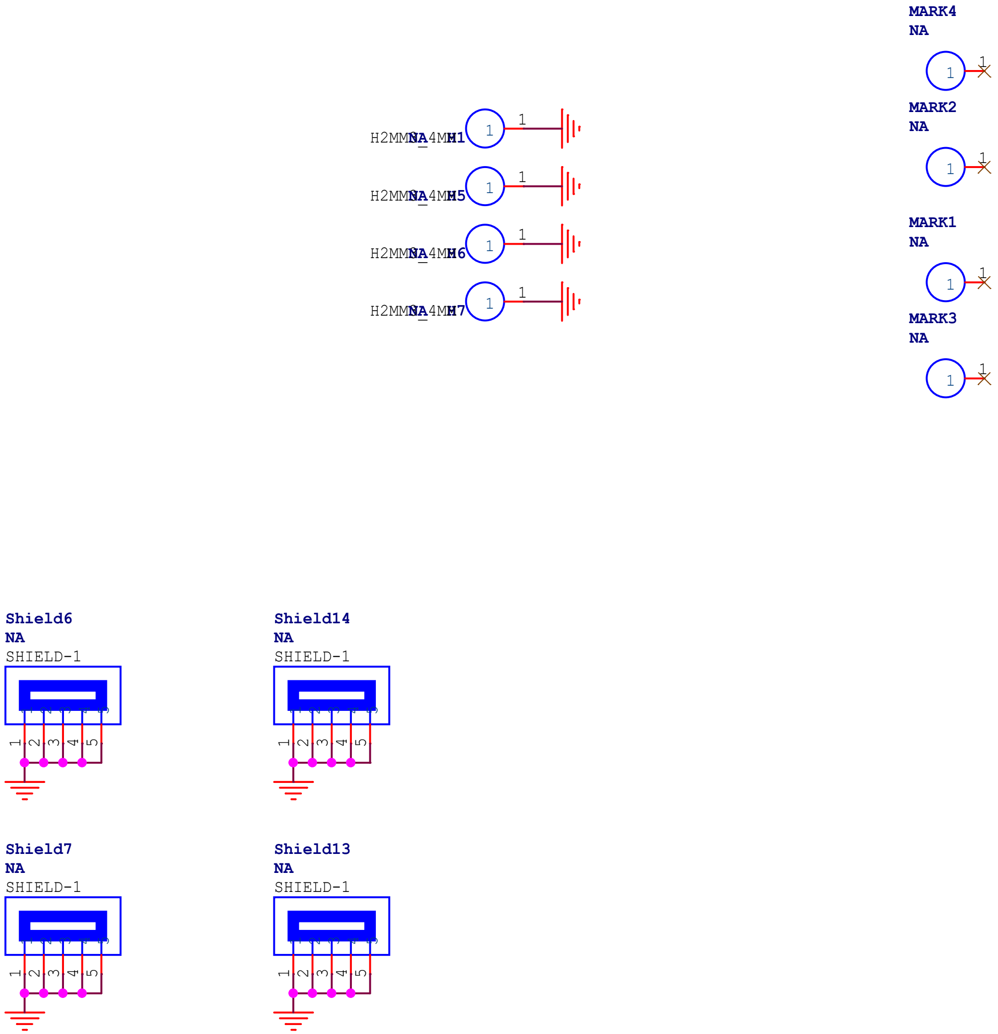
Project:	RK3528_HT2		
File:	21.Key/HW ID/LED		
Date:	Monday, January 29, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	22 of 23



HINLINK

Project:	**RK3528_HT2**	HINLINK	
File:	**22.Mark/Hole**		
Date:	Monday, January 29, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	23 of 23