HINLINK			
Project:	HNAS	HINLINK	
File:	01.Cover Page		
Date:	Sunday, June 23, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 1

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

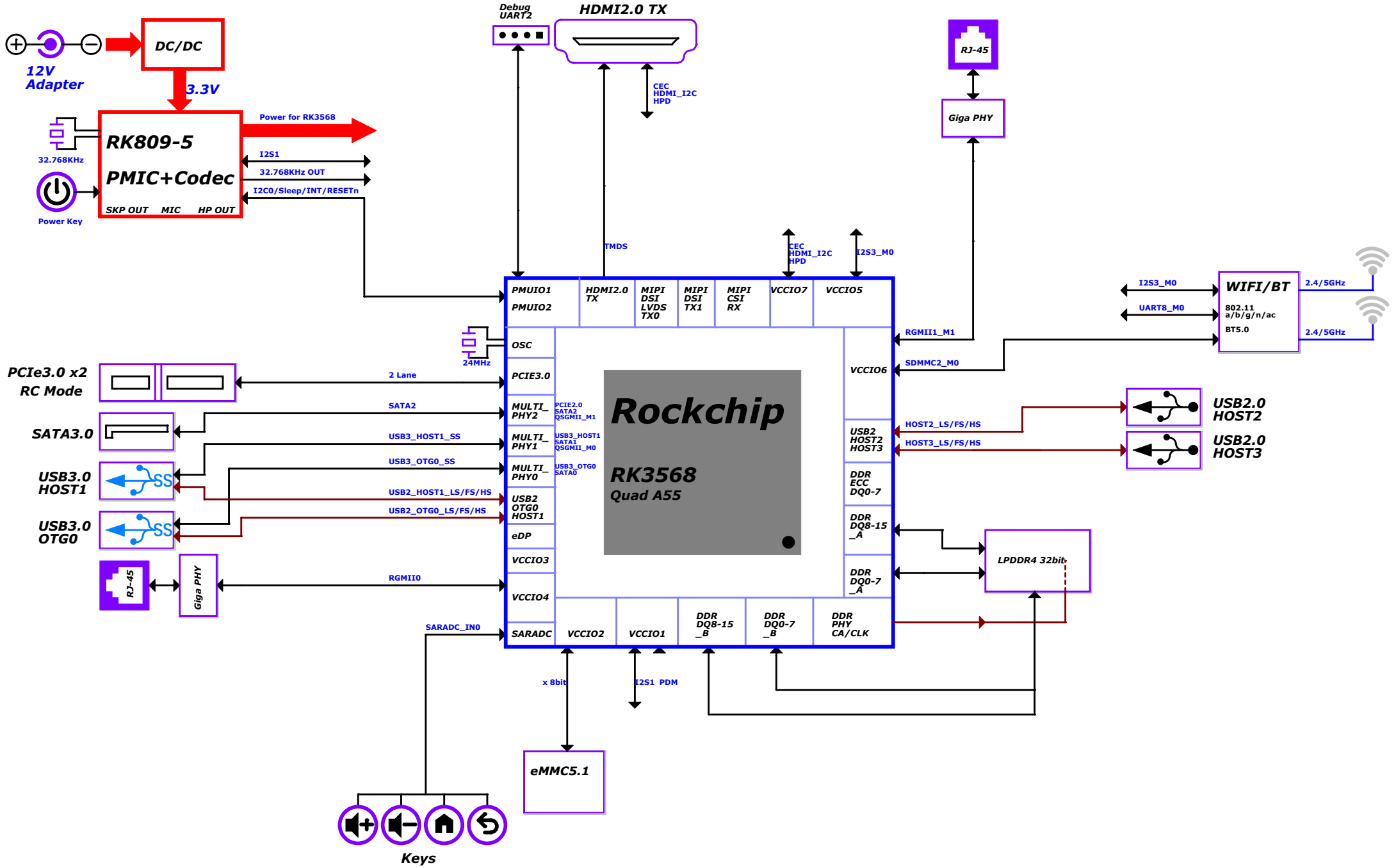
Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

HINLINK			
Project:	HNAS	HINLINK	
File:	02.Index and Notes		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 2

RK3568 Ref Block Diagram



HINLINK		
Project:	HNAS	
File:	03.Block Diagram	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 3

Power Diagram

12V Adapter

DC/DC 3000mA Seq:0 Max:

VCC3V3_SYS

RK809-5

Power on Sequence

VCC1	BUCK1 0.5V~2.4V, 2.5A max	Seq:1	VDD_LOGIC Max:	RK3568_Logic	
VCC2	BUCK2 0.5V~2.4V, 2.5A max	Seq:2	VDD_GPU Max:	RK3568_GPU	
VCC3	BUCK3 0.5V~2.4V, 1.5A max	Seq:3	VCC_DDR Max:	RK3568_DDR_VDDQ	
VCC4	BUCK4 0.5V~3.4V, 1.5A max	OFF	VDD_NPU Max:	RK3568_NPU	
	LDO1 0.6V~3.4V, 400mA max	OFF	VDDA0V9_IMAGE Max:	VDDA0V9_IMAGE	MIPI_CSI_RX_AVDD_0V9 Max: MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 Max: MIPI_DSI_TX1_AVDD_0V9 Max: EDP_TX_AVDD_0V9 Max: HDMI_TX_AVDD_0V9 Max:
VCC5	LDO2 0.6V~3.4V, 400mA max	Seq:1	VDDA_0V9 Max:	VDDA_0V9	SYSPLL_AVDD_0V9 Max: USB2_AVDD_0V9 Max: USB3_AVDD_0V9 Max: MULTI_PHY_AVDD_0V9 Max: PCIE30_AVDD_0V9 Max:
	LDO3 0.6V~3.4V, 100mA max	Seq:1	VDDA0V9_PMU Max:	VDDA0V9_PMU	PMU_VDD_LOGIC_0V9 Max: PMUPLL_AVDD_0V9 Max:
	LDO4(Codec VDDIO) 0.6V~3.4V, 400mA max	OFF	VCCIO_ACODEC Max:	VCCIO1--I2S1/PDM MIC	
VCC6	LDO5 0.6V~3.4V, 400mA max	Seq:4	VCCIO_SD Max:	VCCIO3--SDMMC0	
	LDO6 0.6V~3.4V, 400mA max	Seq:2	VCC3V3_PMU Max:	PMUIO1/ PMUIO2	
	LDO7 0.6V~3.4V, 400mA max	Seq:2	VCCA_1V8 Max:	VCCA_1V8	SYSPLL_AVDD_1V8 Max: USB2_AVDD_1V8 Max: USB3_AVDD_1V8 Max: MULTI_PHY_AVDD_1V8 Max: PCIE30_AVDD_1V8 Max: SARADC_AVDD_1V8 Max:
VCC7	LDO8 0.6V~3.4V, 400mA max	Seq:2	VCCA1V8_PMU Max:	PMUPLL_AVDD_1V8	
	LDO9 0.6V~3.4V, 400mA max	OFF	VCCA1V8_IMAGE Max:	VCCA1V8_IMAGE	MIPI_CSI_RX_AVDD_1V8 Max: MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 Max: MIPI_DSI_TX1_AVDD_1V8 Max: EDP_TX_AVDD_1V8 Max: HDMI_TX_AVDD_1V8 Max:
VCC8	Switch2 2.1 A max, Rdson=100mΩ	Seq:4	VCC3V3_SD Max:	Micro SD Card	
VCC9	Switch1 2.1 A max, Rdson=90mΩ	Seq:4	VCC_3V3 Max:	VCC_3V3	USB3_AVDD_3V3 Max: USB2_AVDD_3V3 Max: VCCIO5,VCCIO7 Max: eMMC_VCC / Nand_VCC Max: VCC3V3_PHY0/1 Max: VCC3V3_TP Max: VCC3V3_SPDIF Max: VCC3V3_WL_VBAT Max: Sensor/IR Receiver Max: UART Device Max: CAN IC Max: MIC Expand Board Max: RGMII/CIF/EBC Expand Board Max: MIC(Option) Max: FSUSB30MUX Max: Max:
	BUCK5: 1.5V~3.6V, 2.5 A max	Seq:2	VCC_1V8 Max:	VCC_1V8	OTP_VCC18 Max: VCCIO2(Default) --eMMC/Nand IO Max: VCCIO4(Default) --WIFI/BT IO Max: VCCIO5(Default) Max: VCCIO6(Default) Max: GIGa PHY0/1 IO Max:
VCC_RTC					

VCC5V0_SYS

EXT DC/DC ,5A Seq:2A — VDD_CPU Max: — RK3568_CPU

EXT LDO ,0.3A Seq:2A — VCC2V5_DDR Max: — DDR4 DRAM

VCC3V3_SYS — Mos-->LCD Panel Max: / Mos-->VCC3V3_VGA Max: / RTC IC Max:

MOS OFF — PCIe Slot Max: / SATA Max:

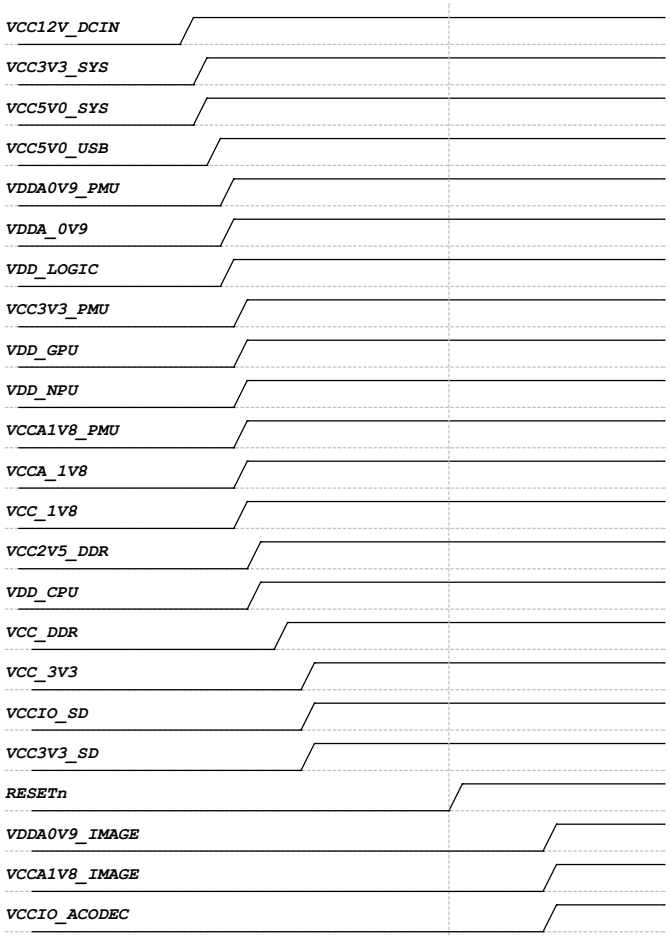
DC/DC 3000mA Seq:0 — VCC5V0_USB Max: — SATA Max: / USB HOST Max:

DC/DC 3000mA Seq:0 — VCC5V0_SYS Max: — VCC5V_HDMI_TX Max: / RK809_SPK_PA Max: / CAN transceiver IC Max: / MIPI-CSI_RX_CON Max: / MIPI/LVDS_Panel_CON0/1 Max: / eDP_Panel_CON/VGA OUT Max: / MIC Expand Board Max: / RGMII/CIF/EBC Expand Board Max: / MOS → VCC5V0_VGA Max: / LDO → VCC3V3_PI6C Max: / LDO → VCC3V3_BU Max:

DC/DC 3000mA — VCC3V3_PCIE Max:

HINLINK		
Project:	HNAS	
File:	04.Power Diagram	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 4

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	OFF	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	ON	TBD	TBD

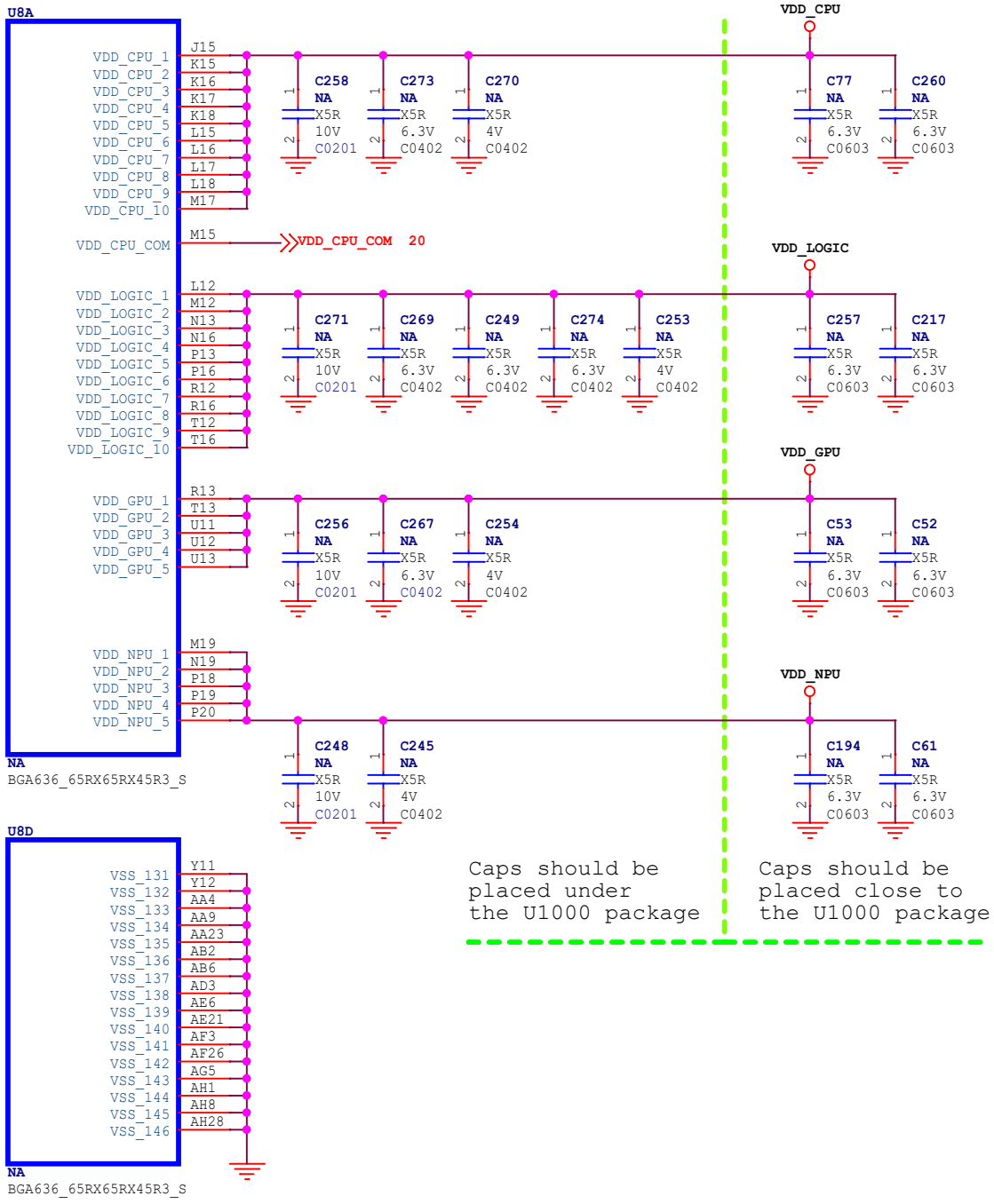
IO Power Domain Map

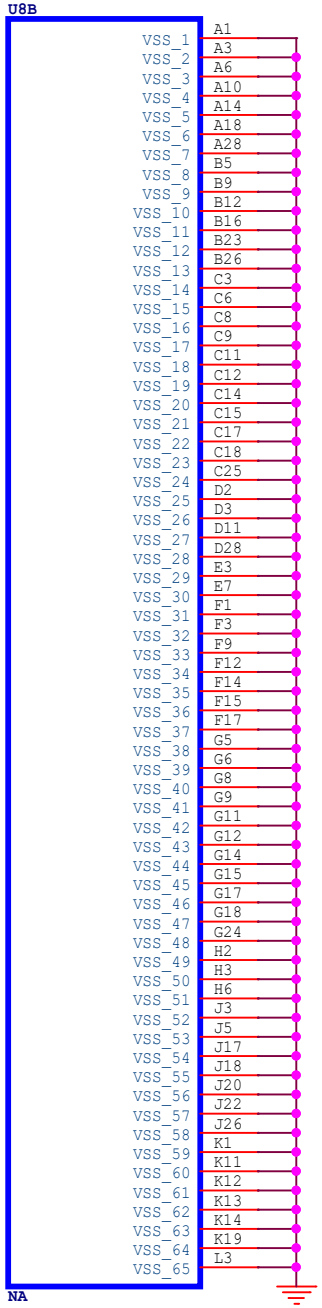
Updates must be Revision accordingly!

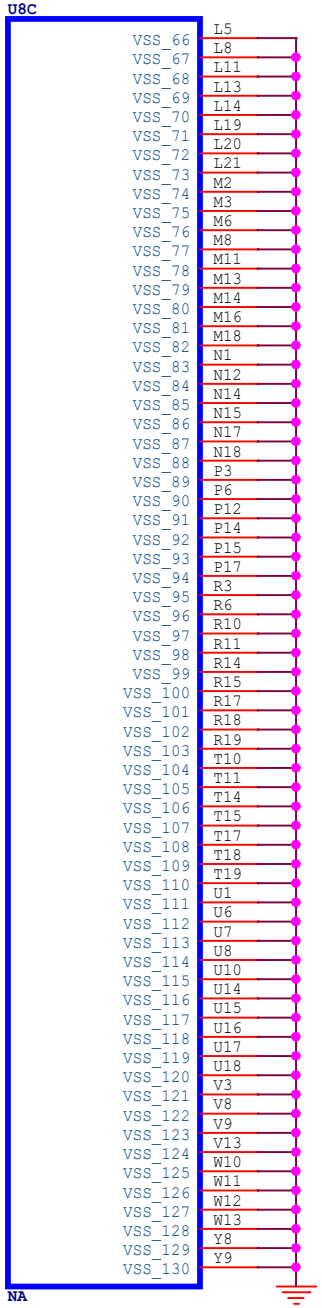
IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

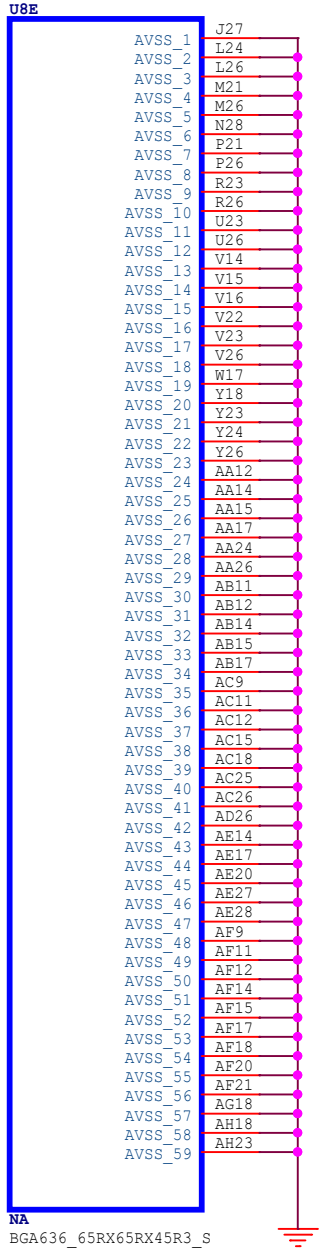
HINLINK			
Project:	HNAS		
File:	05.Power Sequence/IO Domain Map		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 5

RK3568_ABCDE (Power&Gnd)





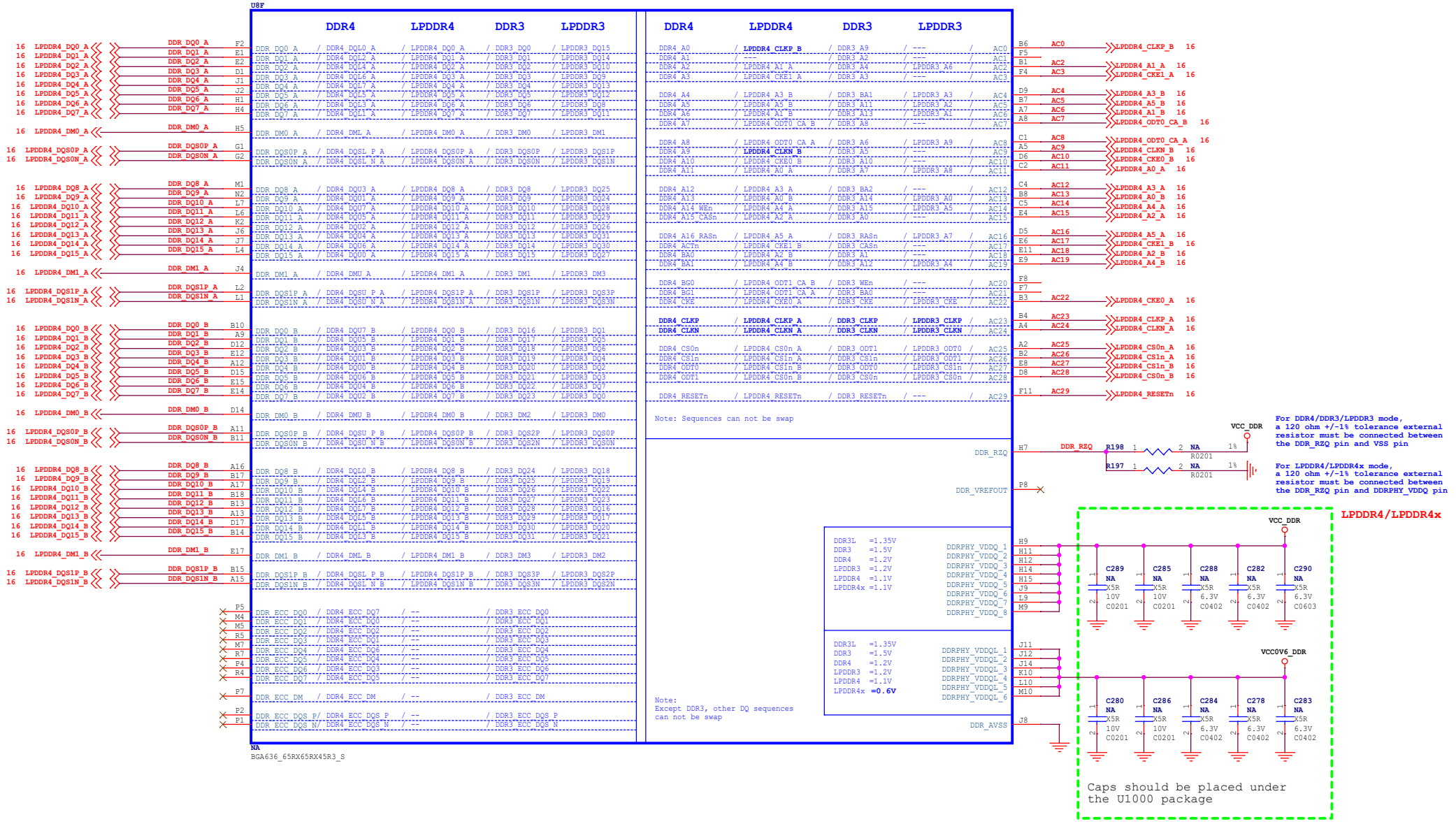




Rockchip Confidential

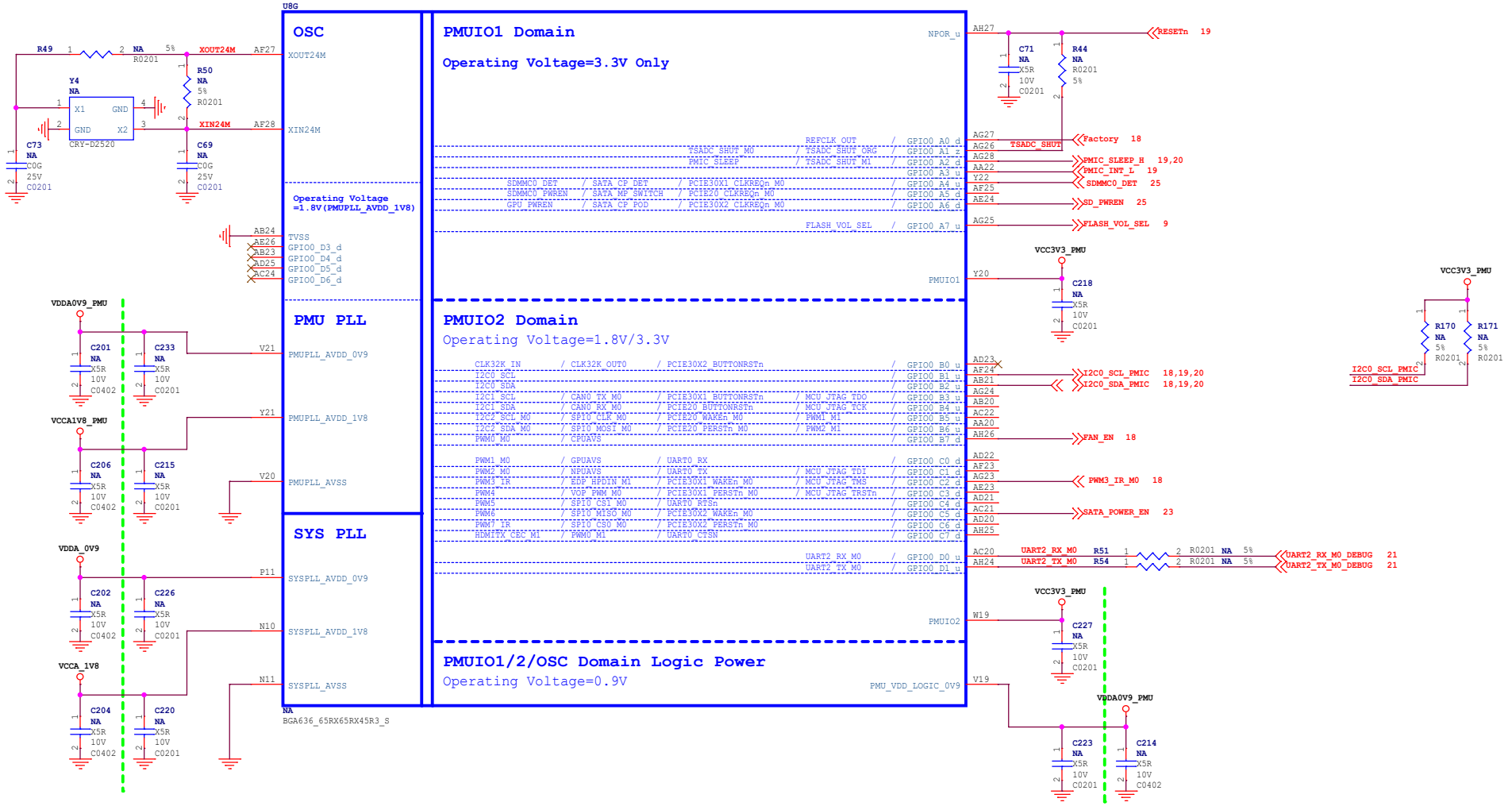
HINLINK		
Project:	HNAS	
File:	06.RK3568_Power/GND	HINLINK
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 6

RK3568_F (DDR PHY)



HINLINK			
Project:	HNAS		
File:	07.RK3568_DDR PHY		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 7

RK3568_G(OSC/PLL/PMUIO1/2)

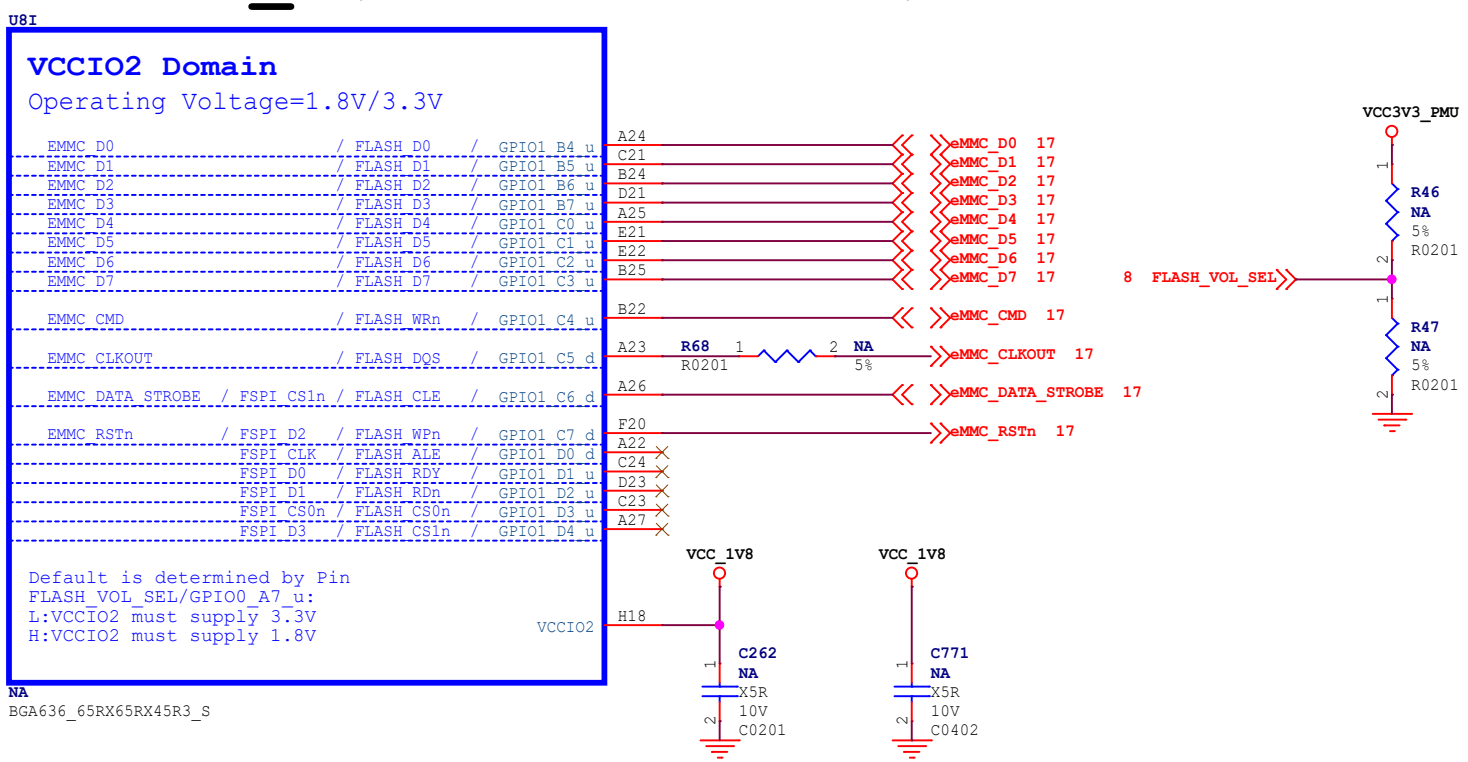


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

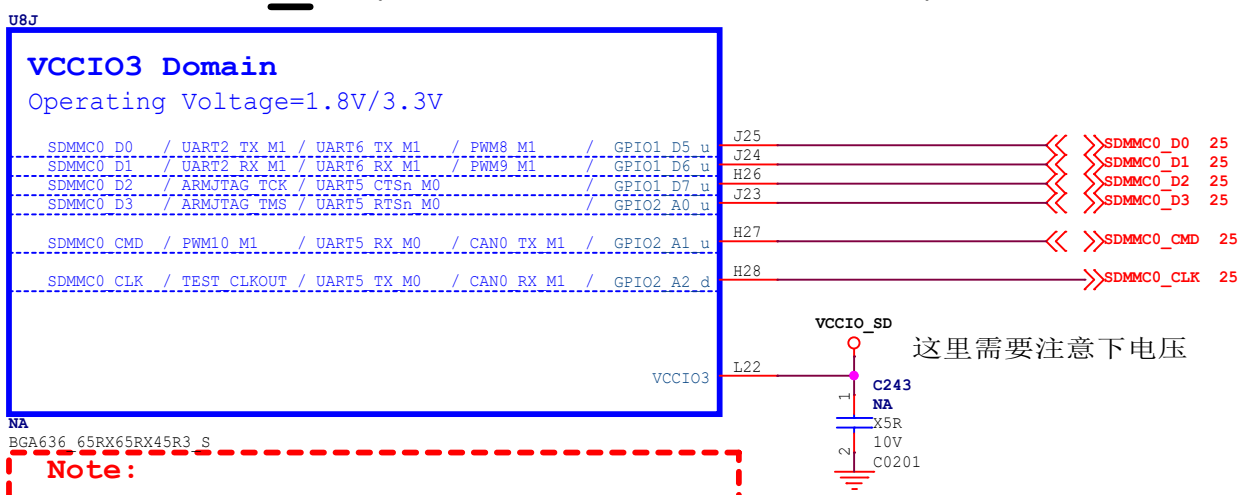
Rockchip Confidential

HINLINK			
Project:	HNAS		
File:	08.RK3568_OSC/PLL/PMUIO		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 8

RK3568_I(VCCIO2 Domain)



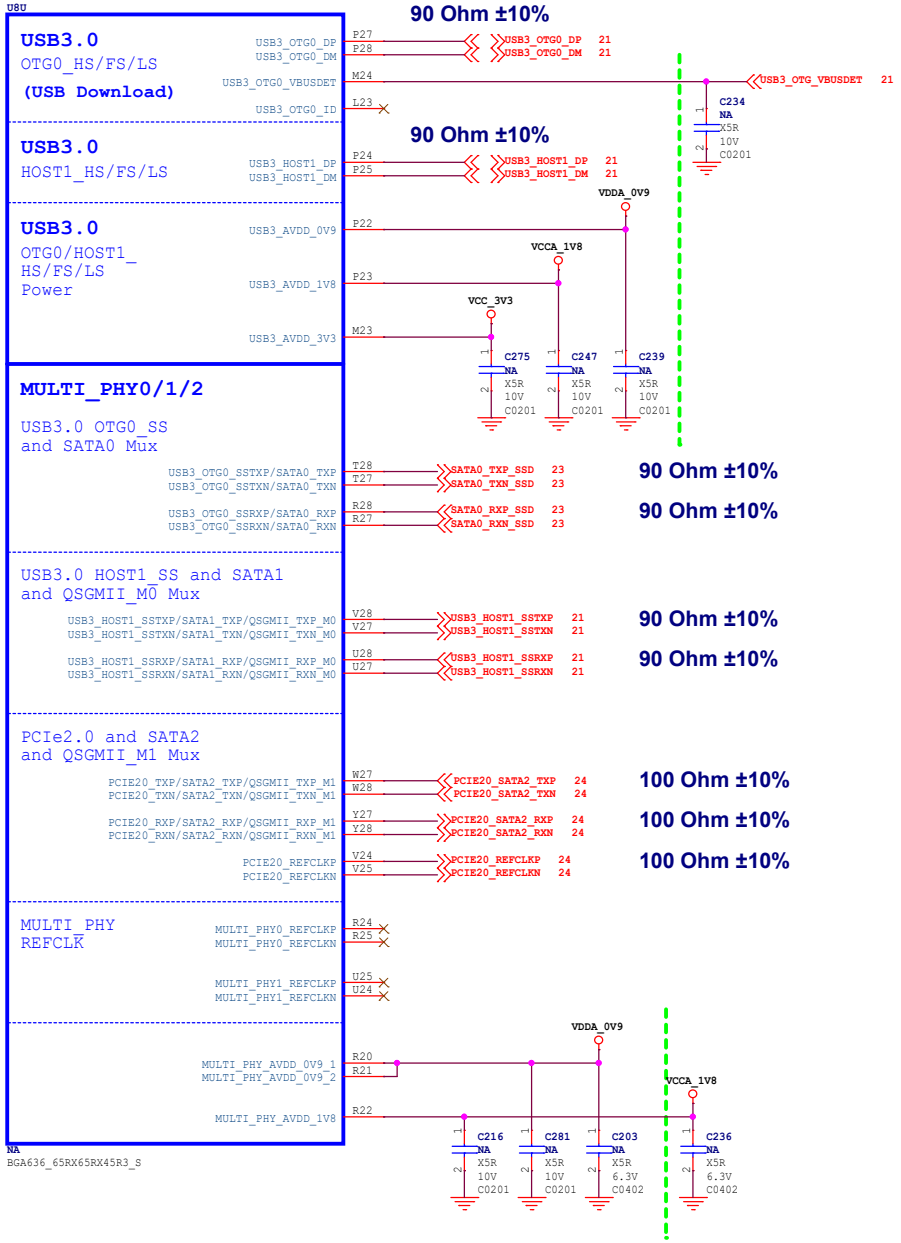
RK3568_J(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

HINLINK			
Project:	HNAS		
File:	09.RK3568_Flash/SD Controller		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 9

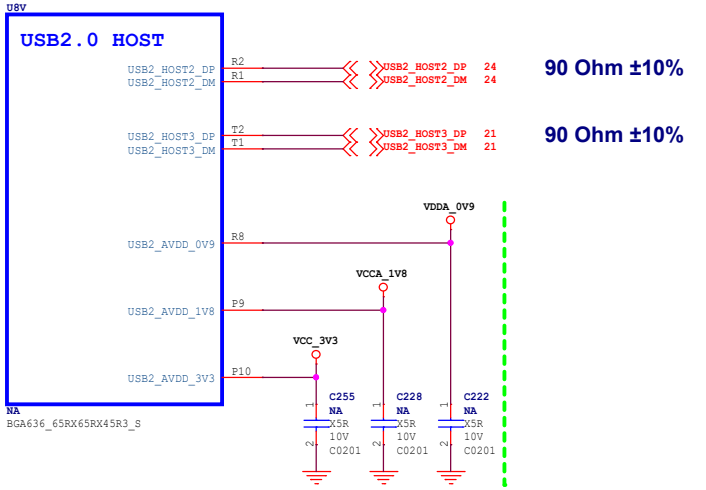
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



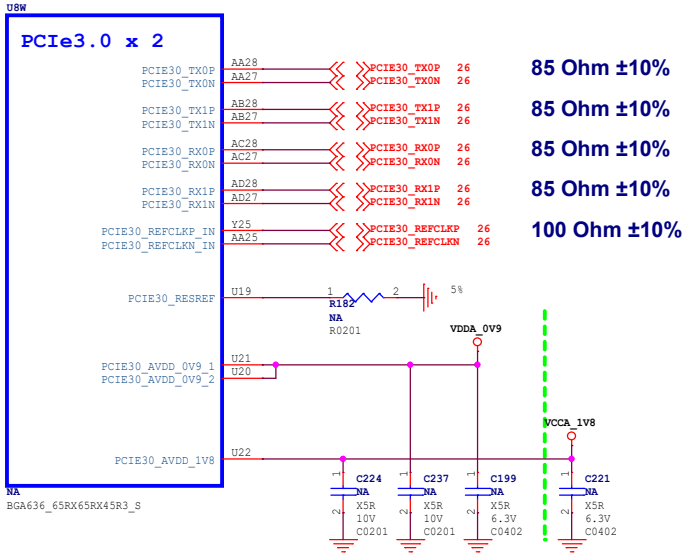
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_V(USB2.0 HOST)

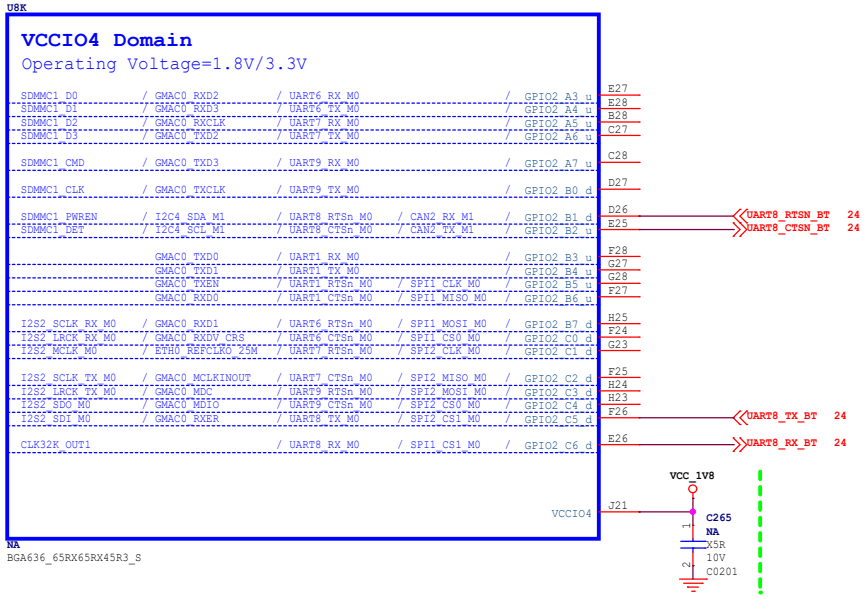


RK3568_W(PCIe3.0 x2)

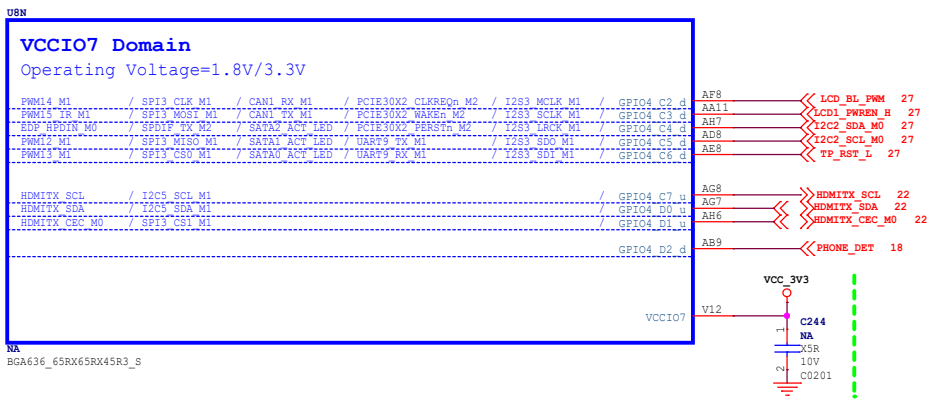


HINLINK			
Project:	HNAS		
File:	10.RK3568_USB/PCIe/SATA PHY		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 10

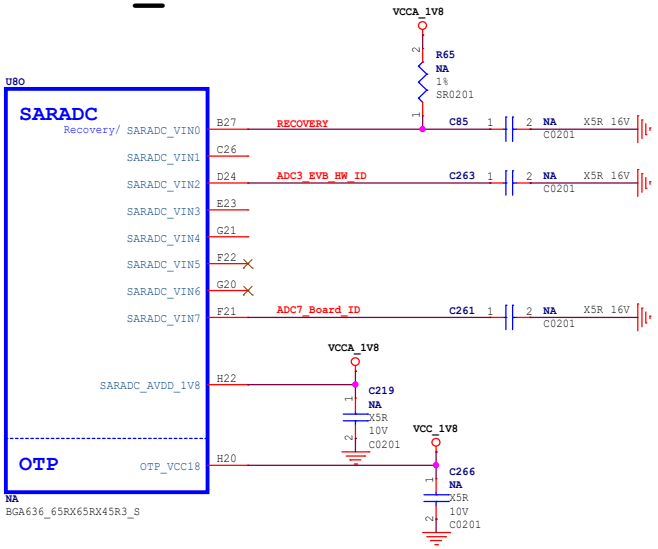
RK3568_K(VCCIO4 Domain)

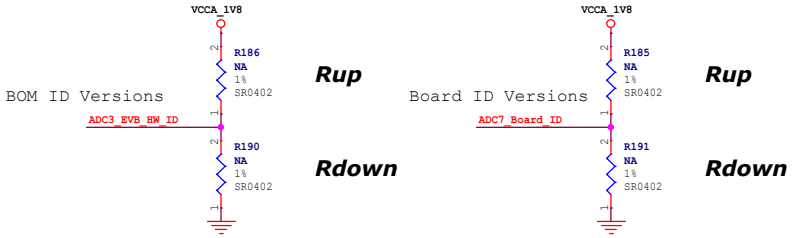


RK3568_N(VCCIO7 Domain)



RK3568_O(SARADC/OTP)





BOM ID Versions TABLE 1

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	100K	2047	0.9V	V3.0
LEVEL4	100K	DNP	4096	1.8V	V4.0

Board ID Versions TABLE 2

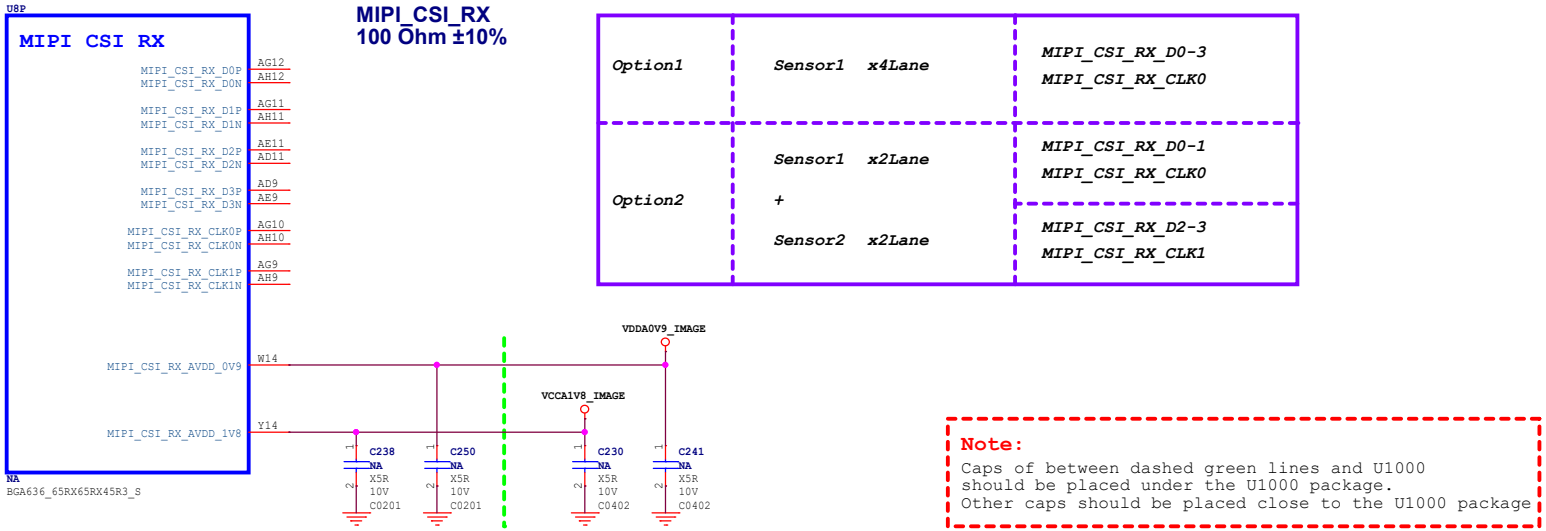
Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	WIFI AP6212+SATA
LEVEL2	100K	20K	682	0.3V	WIFI AP6256+SATA
LEVEL3	100K	100K	2047	0.9V	WIFI WIFI6
LEVEL4	100K	200K	4096	1.2V	WIFI NC+SATA

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

HINLINK

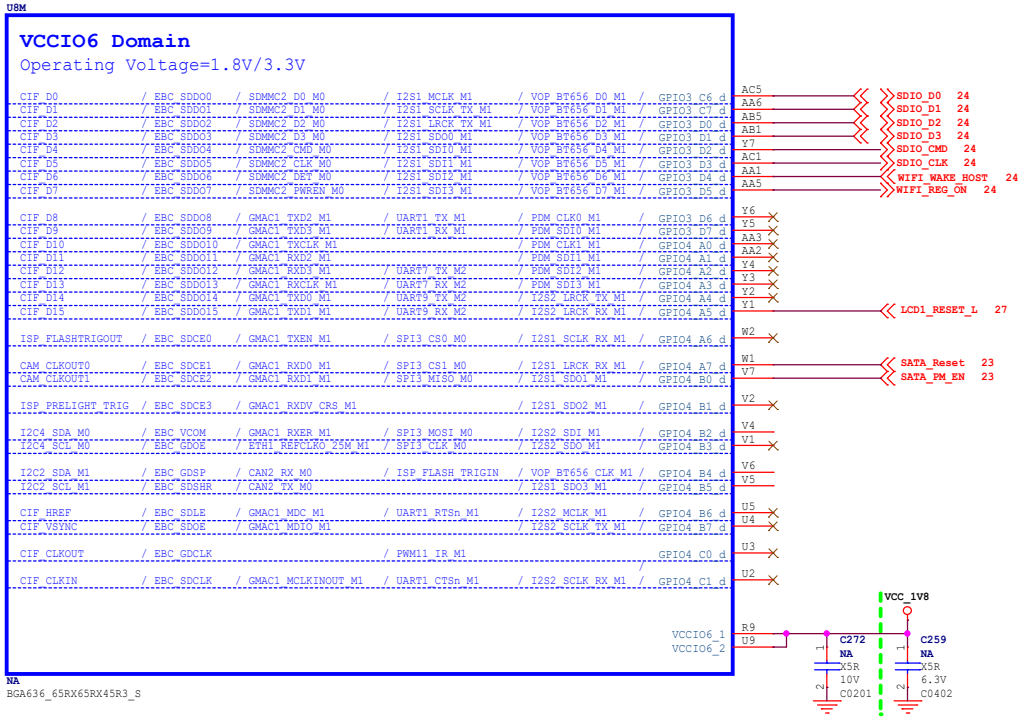
Project:	HNAS		
File:	11.RK3568_SARADC/GPIO		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 11

RK3568_P(MIPI_CSI_RX)



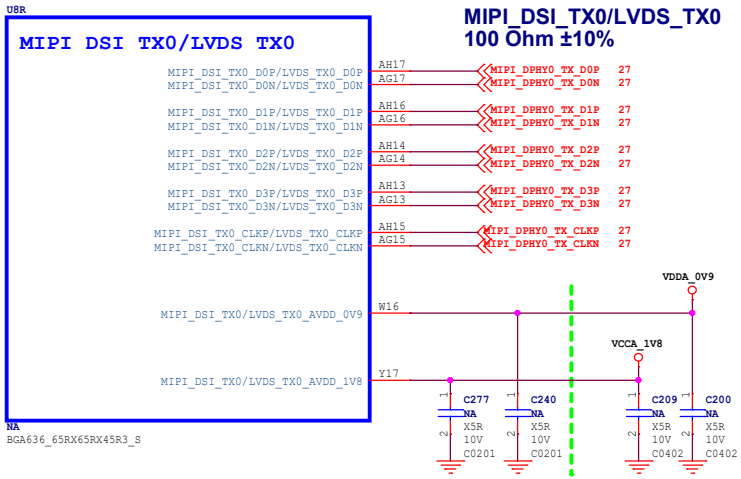
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_M(VCCIO6 Domain)

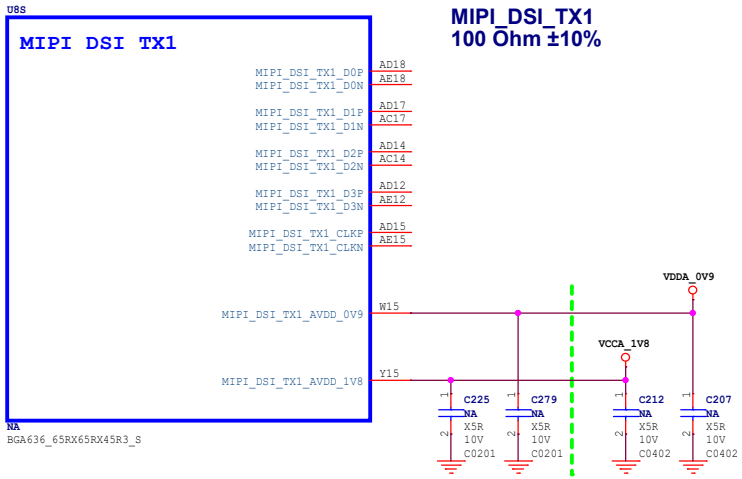


HINLINK		
Project:	HNAS	
File:	12.RK3568_VI Interface	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 12

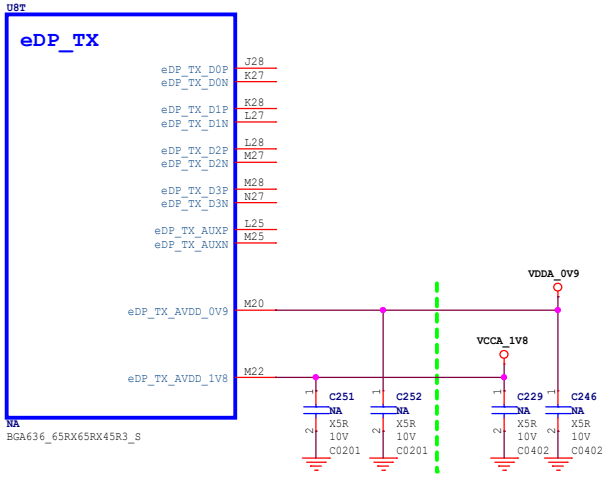
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



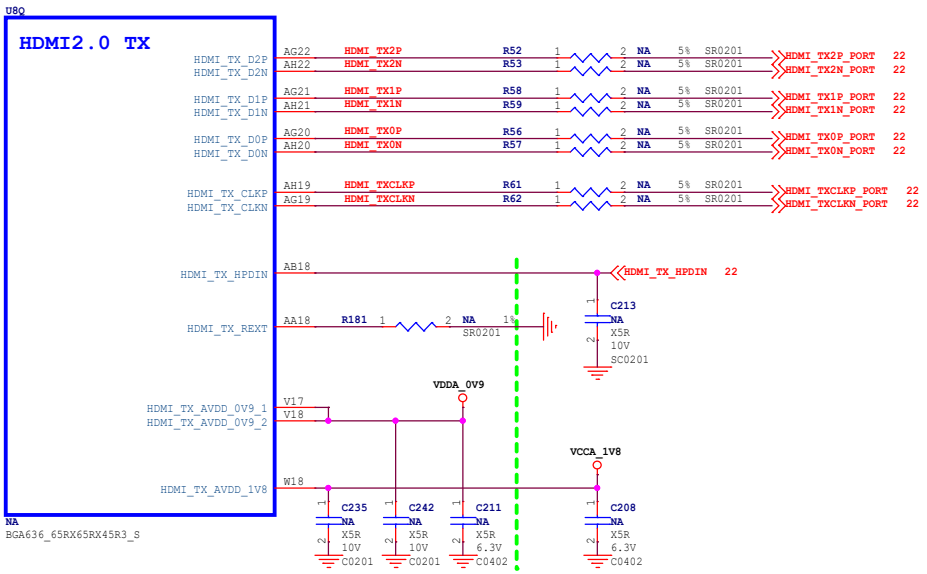
RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_Q(HDMI2.0 TX)



HINLINK		
Project:	HNAS	
File:	13.RK3568_VO Interface_1	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 13

RK3568_L(VCCIO5 Domain)

U8L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

NA
BGA636_65RX65RX45R3_S

AG6 — 25GLAN_ResetA 26
AD7
AC8
AC7
AF5 — PCIE30X2_CLKREQn_M1_3V3 24
AF6 — PCIE30X2_WAKEn_M1_3V3 24
AD6 — PCIE30X2_PERSTn_M1_3V3 24
AH5
AH4 — BT_REG_ON 24
AB8 — BT_WAKE_HOST 24
AE5 — HOST_WAKE_BT 24
AG4
AF4 — 25GLAN_ResetB 26
AH3 — Green_LED
AG3
AH2 — NET_LED
AG2 — WORK_LED
AG1 — SATA3_LED 23
AF2 — SATA2_LED 23
AF1 — I2C5_SCL_3V3 18
AE1 — I2C5_SDA_3V3 18
AE2 — SATA1_LED 23
AE3 — SATA0_LED 23
AD4 — TP1_INT_L 27
AD2 — KEY 24
AD1 — Reset_Zigbee 24
AA7 — UART5_TX_Zigbee 24
AC4 — UART5_RX_Zigbee 24
AC3 — PWM_LED
AC2

VCC_3V3
V10, V11 — VCCIO5_1, VCCIO5_2
C264 NA X5R 10V C0201
C268 NA X5R 6.3V C0201

VCC3V3_SYS
R87 NA SR0201
D15 NA LED0603W
Green_LED — R202 NA 5% R0201 — 预留 — Q13 NA SOT_323
R204 NA R0201 5%

VCC3V3_SYS
R80 NA SR0201
D14 NA LED0603W
NET_LED — R195 NA 5% R0201 — Q12 NA SOT_323
R199 NA R0201 5%

VCC3V3_SYS
R99 NA SR0201
D16 NA LED0603W
WORK
WORK_LED — R210 NA 5% R0201 — Q14 NA SOT_323
R213 NA R0201 5%

VCC3V3_SYS
R258 NA SR0201
D46 NA LED0603W
POWER
18 POWER_EN — R259 NA 5% R0201 — Q18 NA SOT_323
C393 NA X5R 10V C0201

VCC3V3_SYS
R102 NA 5% R0201
R106 NA SR0201 5%
Q4 NA SOT_323
PWM_LED
VCC5V0_SYS
R105 NA 5% R0201
VCC5V0_SYS
PWM_LED_PORT 18
C119 NA X7R 10V SC0603
C113 NA SC0201 X5R 16V

HINLINK			
Project:	HNAS		
File:	14.RK3568_VO Interface_2		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 14

RK3568_H(VCCIO1 Domain)

U8H

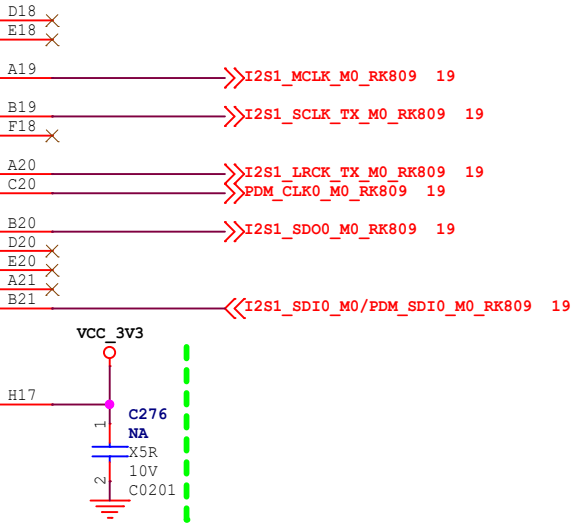
VCCIO1 Domain

Operating Voltage=1.8V/3.3V

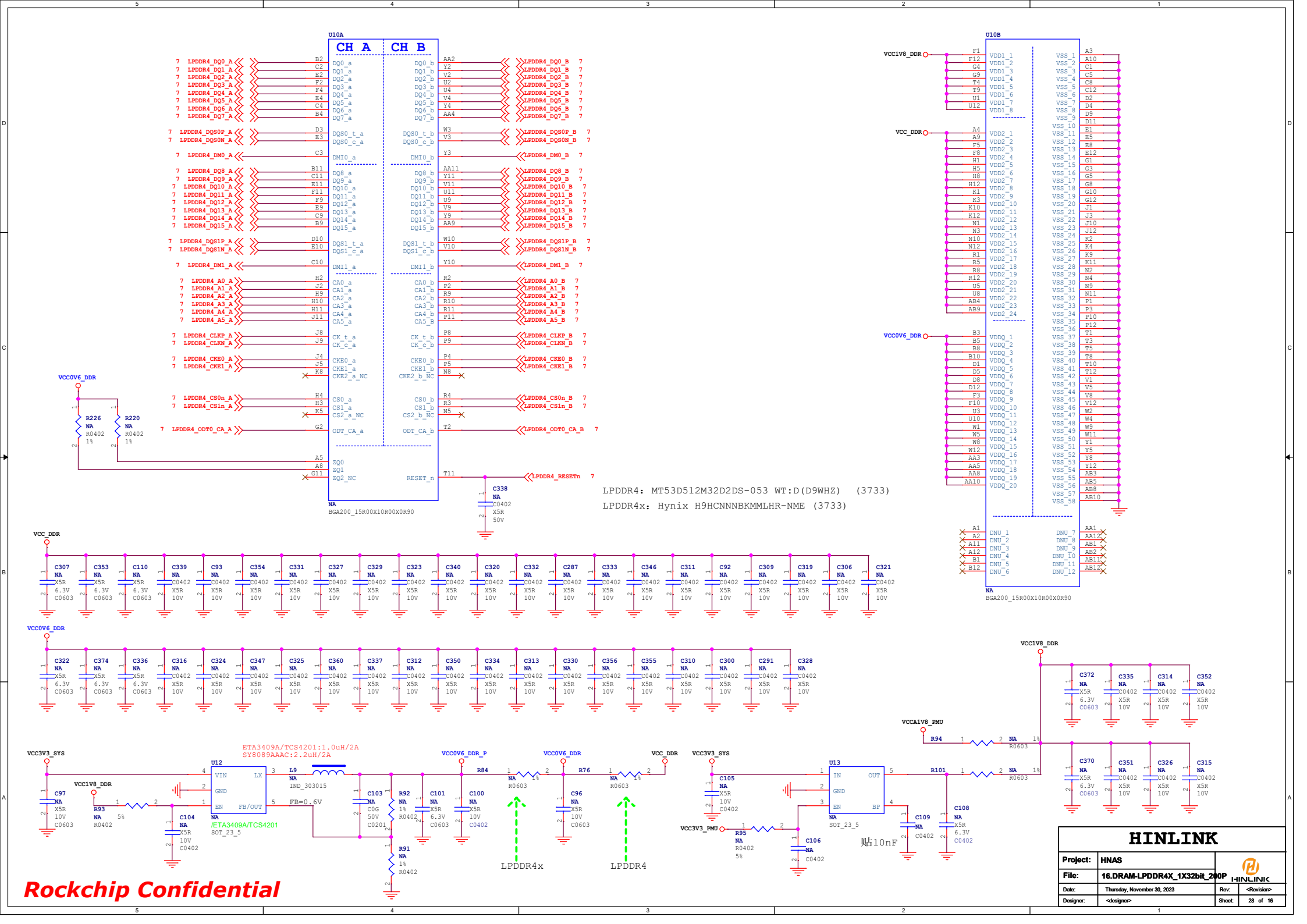
I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u	D18
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u	E18
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/ GPIO1_A2_d	A19
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d	B19
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d	F18
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d	A20
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d	C20
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d	B20
I2S1_SDI1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d	D20
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d	E20
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d	A21
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d	B21
					VCCIO1	H17

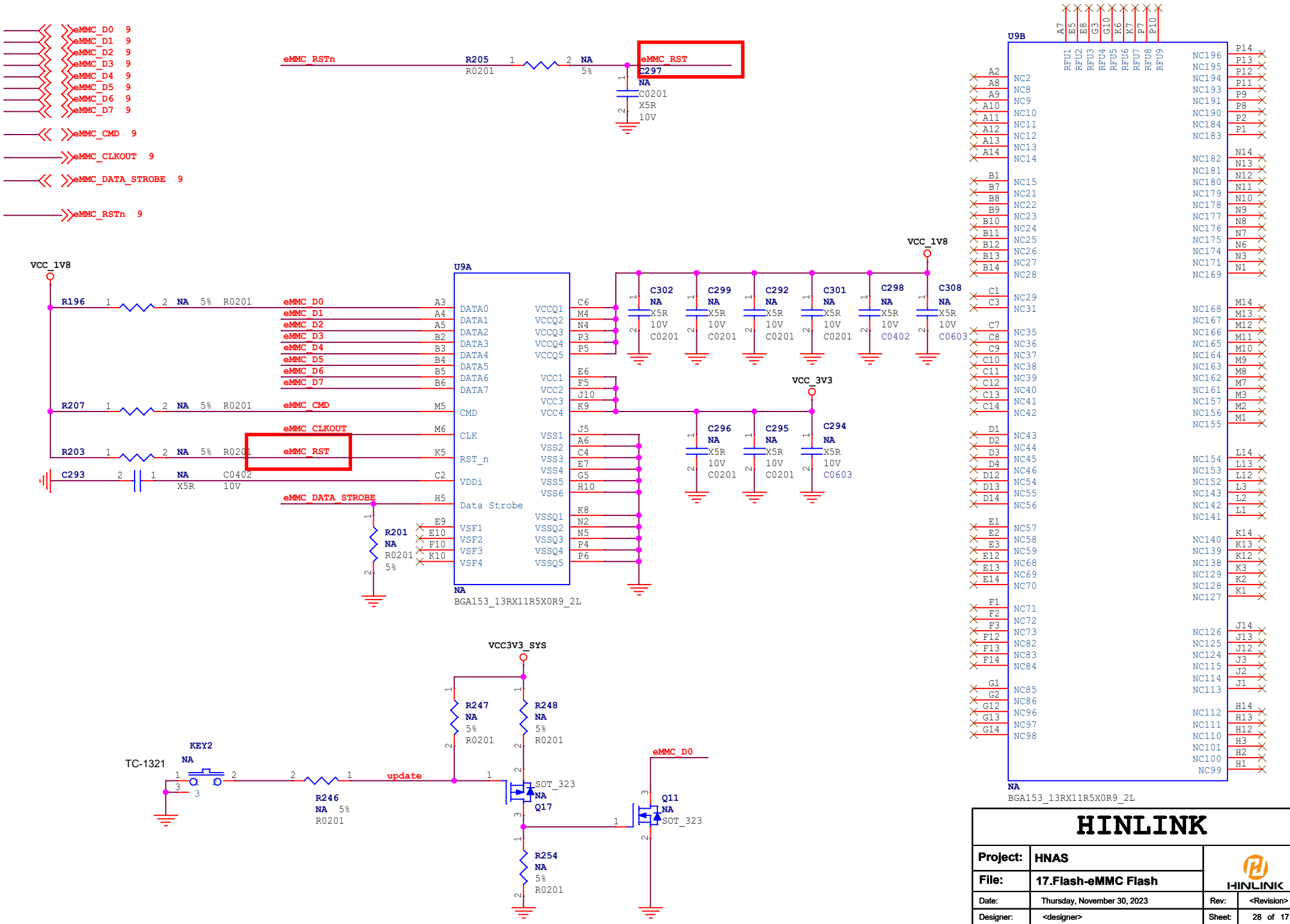
NA

BGA636_65RX65RX45R3_S

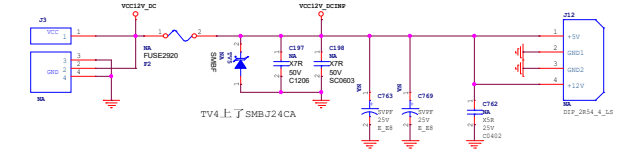


HINLINK			
Project:	HNAS		
File:	15.RK3568_Audio Interface		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 15

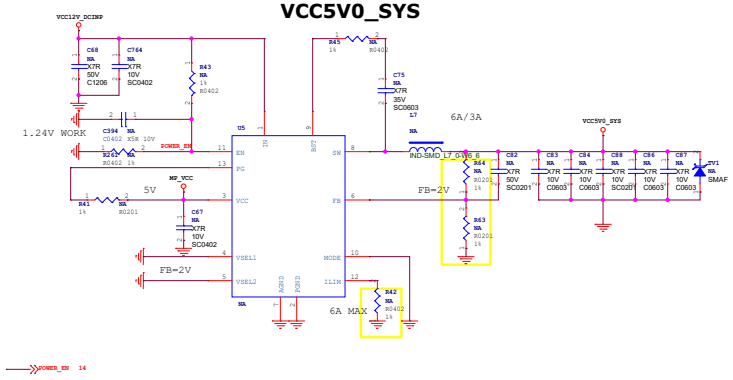

U10A
CH A
CH B
BGA200_15R00X10R00X0R90
U10B
BGA200_15R00X10R00X0R90
LPDDR4: MT53D512M32D2DS-053 WT:D(D9WHZ) (3733)
LPDDR4x: Hynix H9HCNNNBKMMLHR-NME (3733)
VCC_DDR
VCC0V6_DDR
VCC1V8_DDR
VCCA1V8_PMU
VCC3V3_SYS
VCC3V3_PMU
VCC0V6_DDR_P
U12
U13
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
/ETA3409A/TCS4201
FB=0.6V
LPDDR4x
LPDDR4
HINLINK
Project: HNAS
File: 16.DRAM-LPDDR4X_1X32bit_200P
Date: Thursday, November 30, 2023
Rev: <Revision>
Designer: <designer>
Sheet: 28 of 16
Rockchip Confidential


eMMC_D0 9
eMMC_D1 9
eMMC_D2 9
eMMC_D3 9
eMMC_D4 9
eMMC_D5 9
eMMC_D6 9
eMMC_D7 9
eMMC_CMD 9
eMMC_CLKOUT 9
eMMC_DATA_STROBE 9
eMMC_RSTn 9
eMMC_RSTn
R205 R0201 NA 5%
eMMC_RST
C297 NA C0201 X5R 10V
U9B
BGA153_13RX11R5X0R9_2L
VCC_1V8
VCC_3V3
U9A
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7
CMD
CLK
RST_n
VDDi
Data Strobe
VCCQ1 VCCQ2 VCCQ3 VCCQ4 VCCQ5
VCC1 VCC2 VCC3 VCC4
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6
VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5
VSF1 VSF2 VSF3 VSF4
R196 R207 R203 C293
C302 C299 C292 C301 C298 C308
C296 C295 C294
R201 NA R0201 5%
BGA153_13RX11R5X0R9_2L
VCC3V3_SYS
R247 R248 R254 R246
KEY2 TC-1321
update
SOT_323
Q17 Q11
eMMC_D0
HINLINK
Project: HNAS
File: 17.Flash-eMMC Flash
Date: Thursday, November 30, 2023
Designer: <designer>
Rev: <Revision>
Sheet: 28 of 17

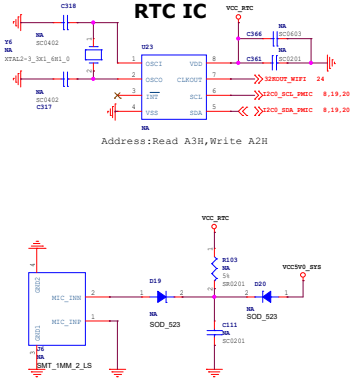
12-24V/3A DCIN



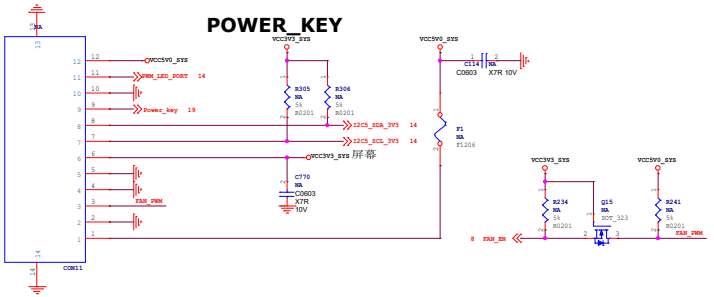
VCC5V0_SYS

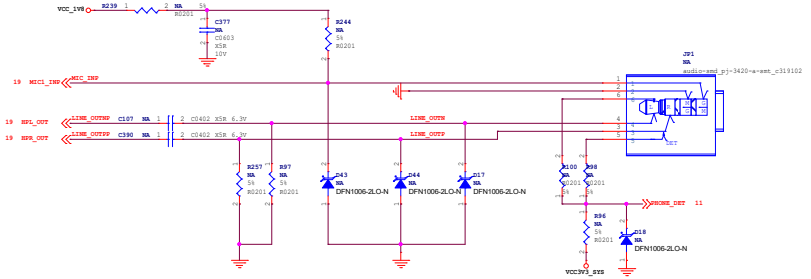


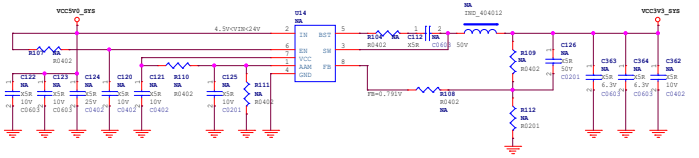
RTC IC

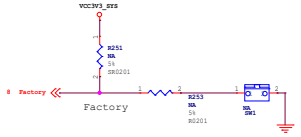


POWER_KEY

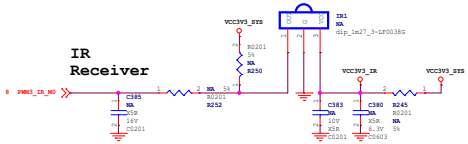








IR Receiver

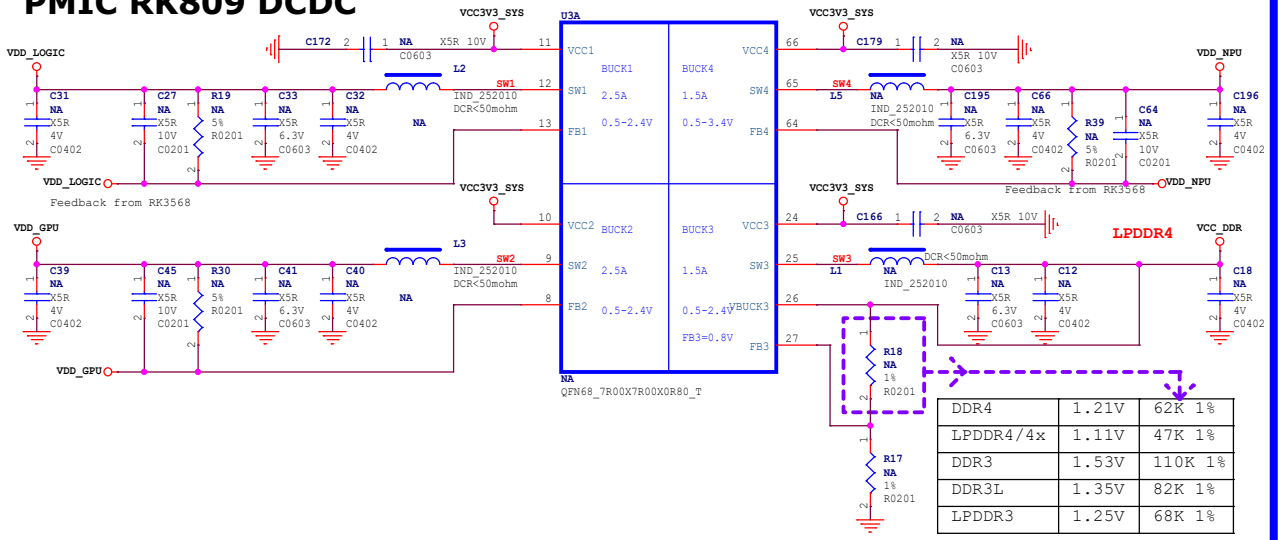


Project:	HNAS
File:	18.Power_DC IN
Date:	Sunday, June 23, 2024
Designer:	<designer>
Rev:	<Revision>
Sheet	28 of 58

HINLINK

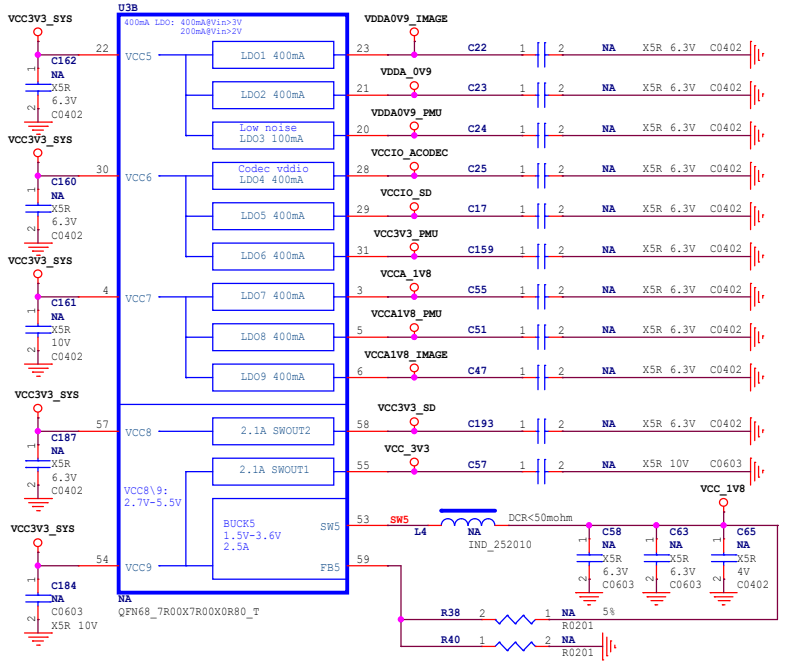
I2C0_SCL_PMIC 8,18,20
I2C0_SDA_PMIC 8,18,20
PMIC_INT_L 8
PMIC_SLEEP_H 8,20
RESETn 8,19

PMIC RK809 DCDC

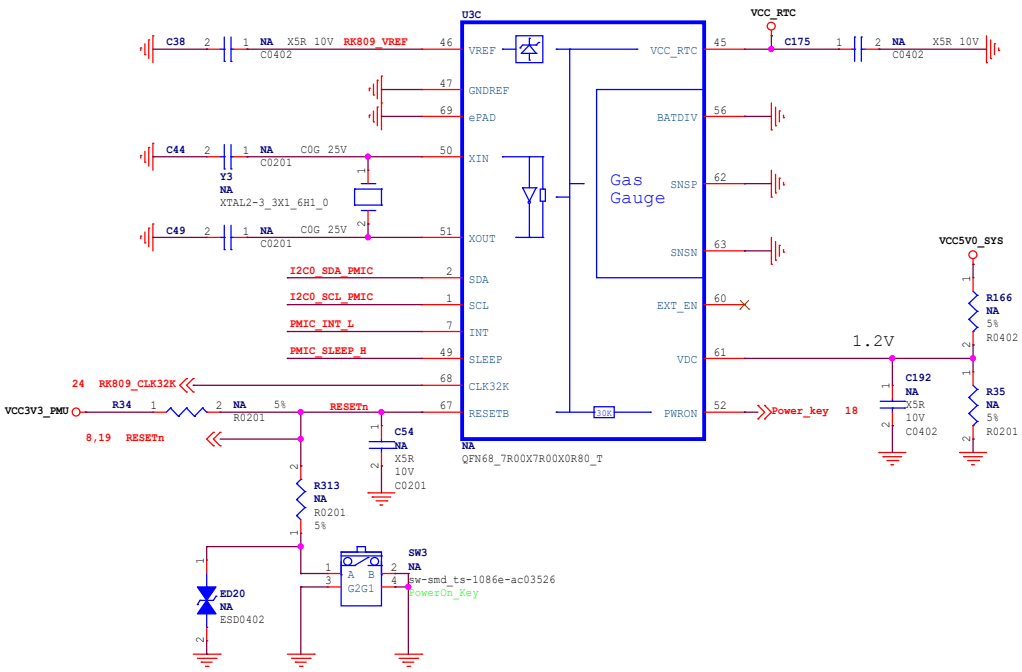


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

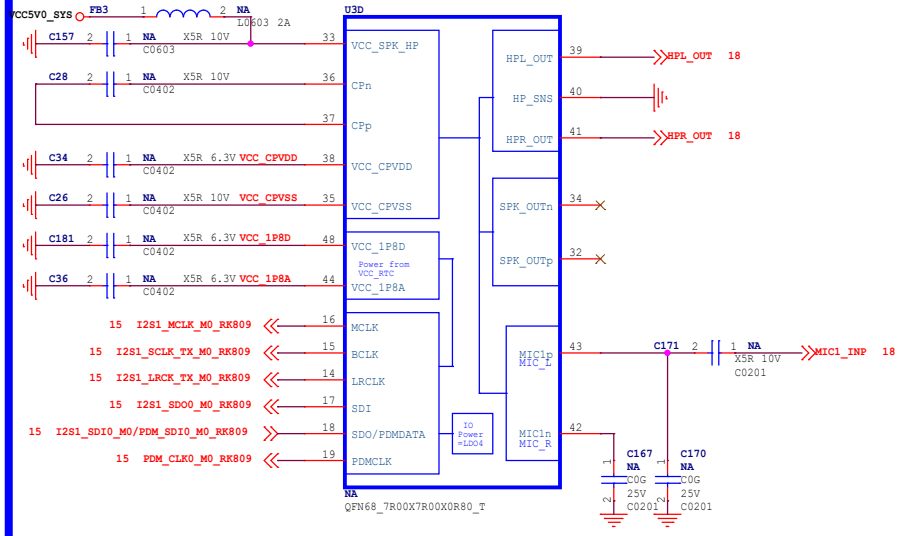
PMIC RK809 LDO



PMIC RK809 Managerment



PMIC RK809 CODEC

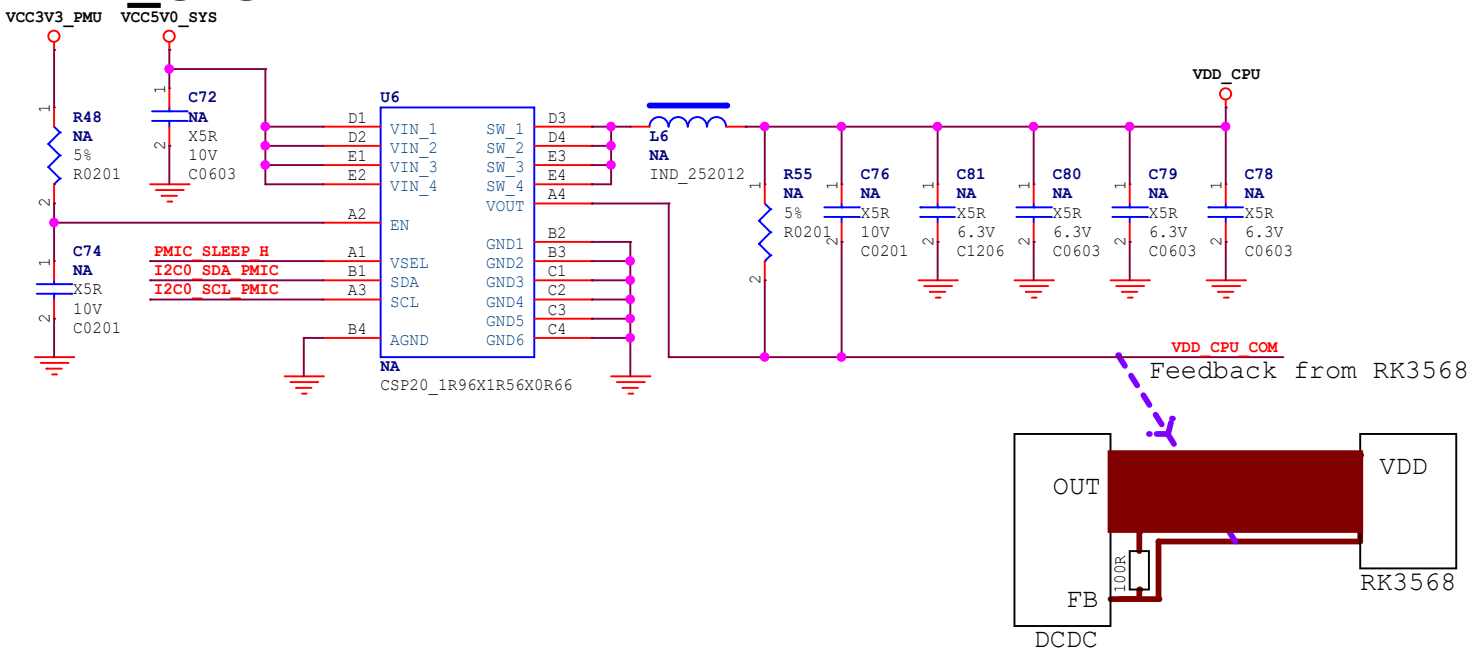


HINLINK			
Project:	HNAS		
File:	19.Power_PMIC		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 19

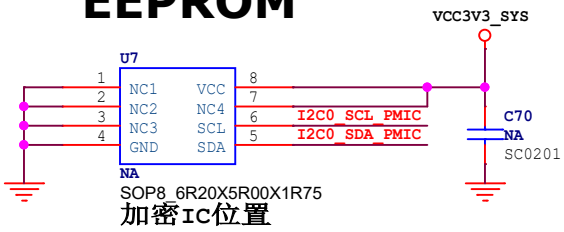
PMIC_SLEEP_H 8,19
VDD_CPU_COM 6

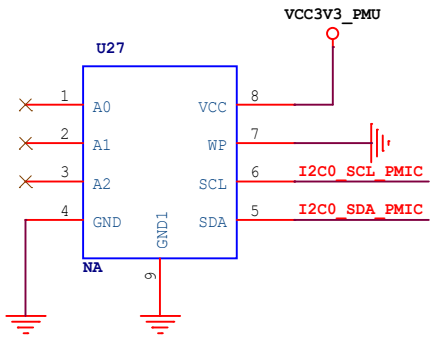
I2C0_SCL_PMIC 8,18,19
I2C0_SDA_PMIC 8,18,19

VDD_CPU



EEPROM

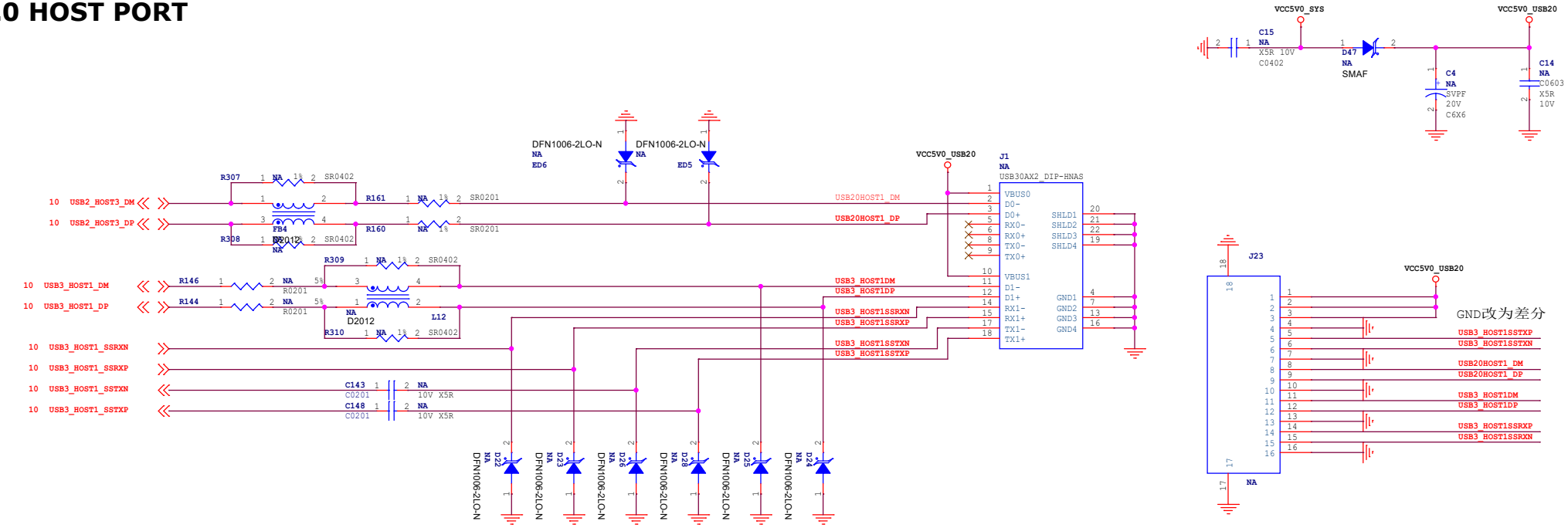




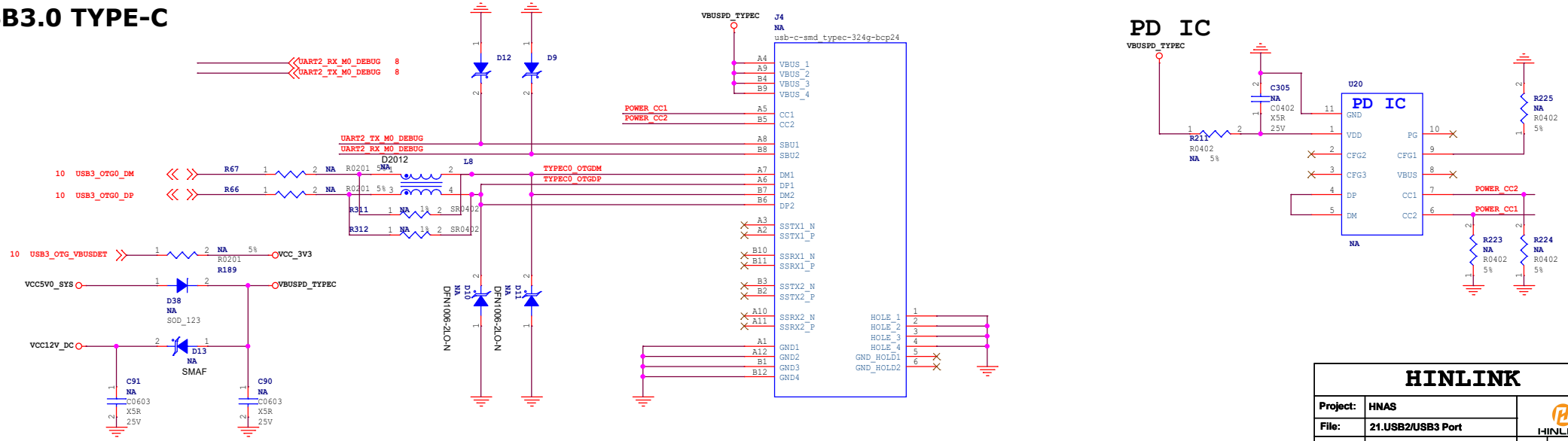
HINLINK			
Project:	HNAS		
File:	20.Power_other		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 20

USB2.0 HOST PORT

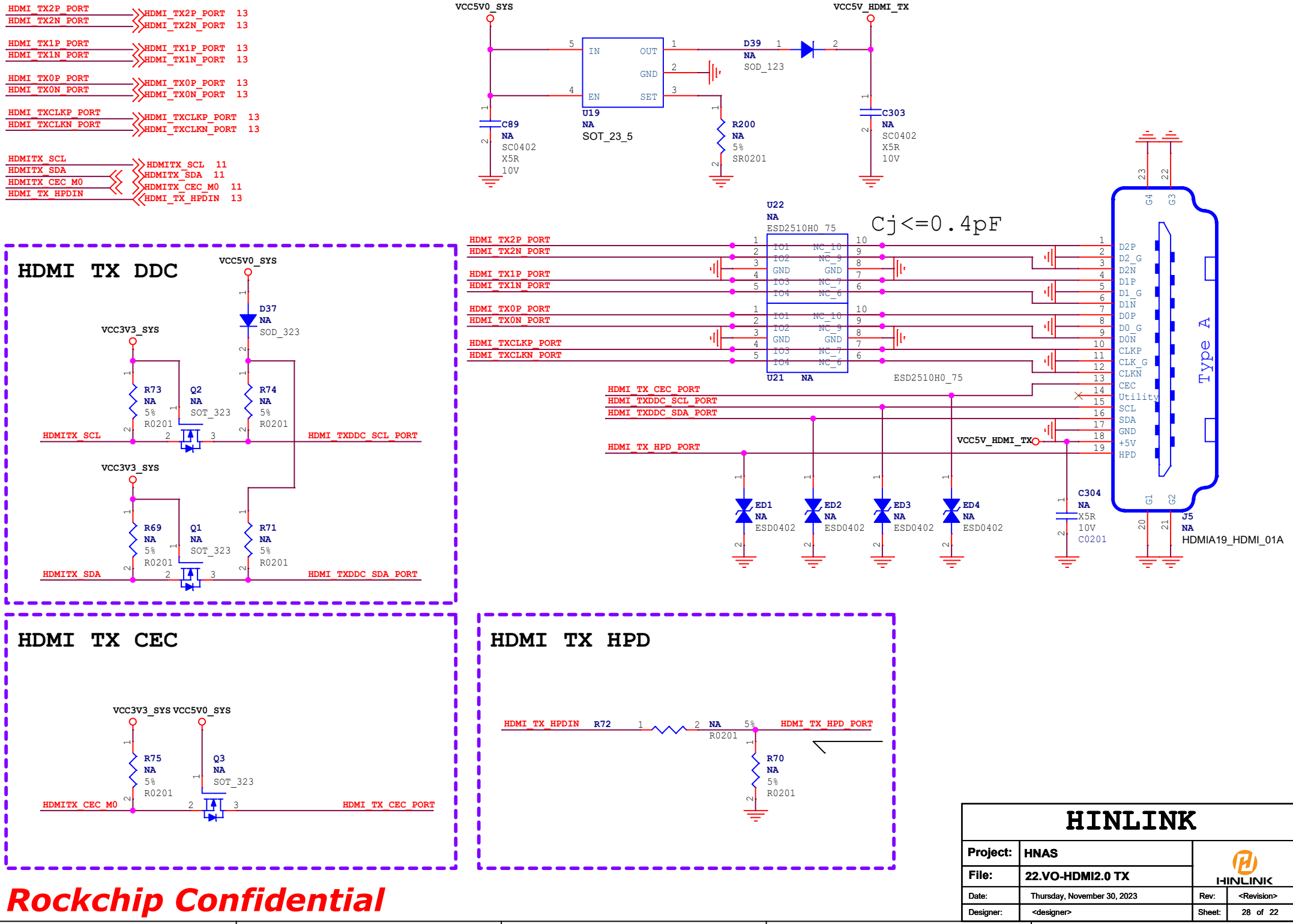
USB3.0 HOST PORT



USB3.0 TYPE-C

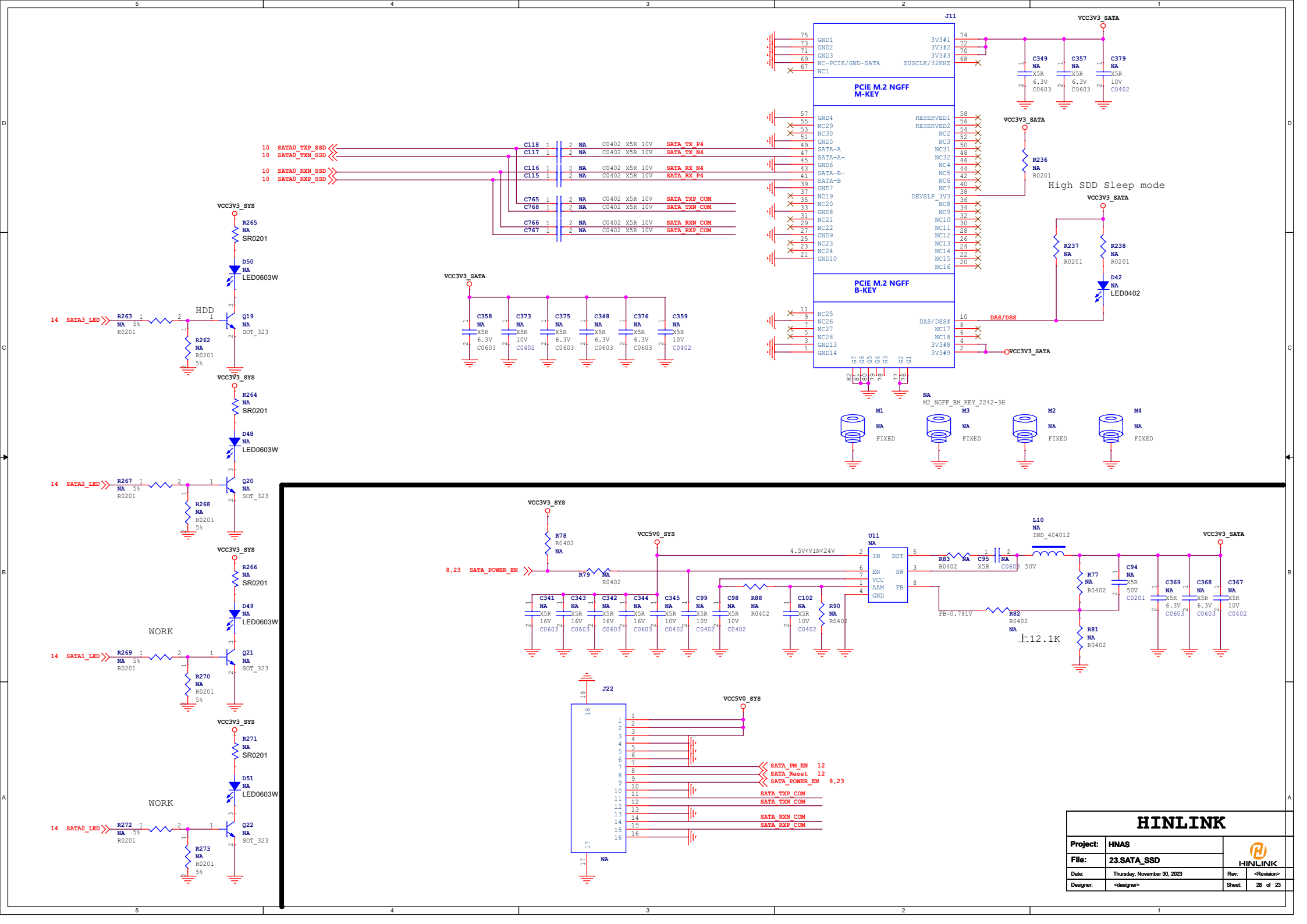


HINLINK		
Project:	HNAS	
File:	21.USB2/USB3 Port	
Date:	Friday, December 01, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 21



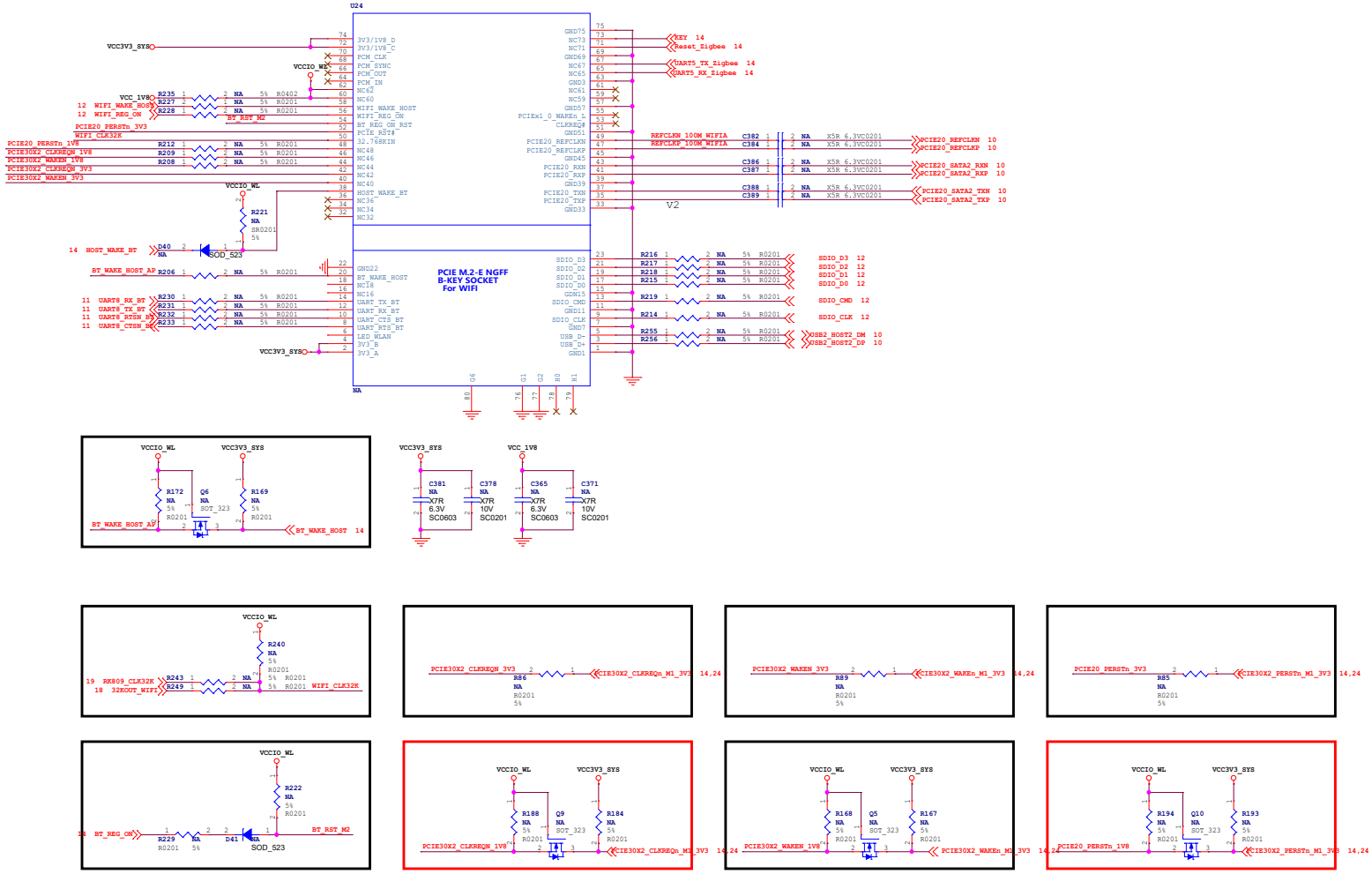
Rockchip Confidential

HINLINK		
Project:	HNAS	
File:	22.VO-HDMI2.0 TX	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 22

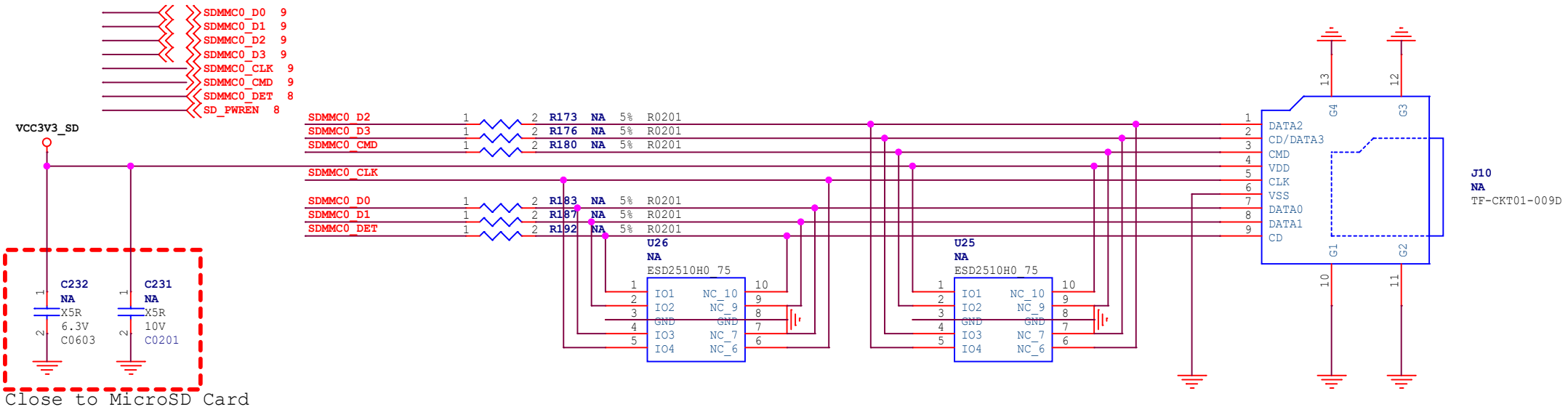


HINLINK			
Project:	HNAS		
File:	23.SATA_SSD		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 23

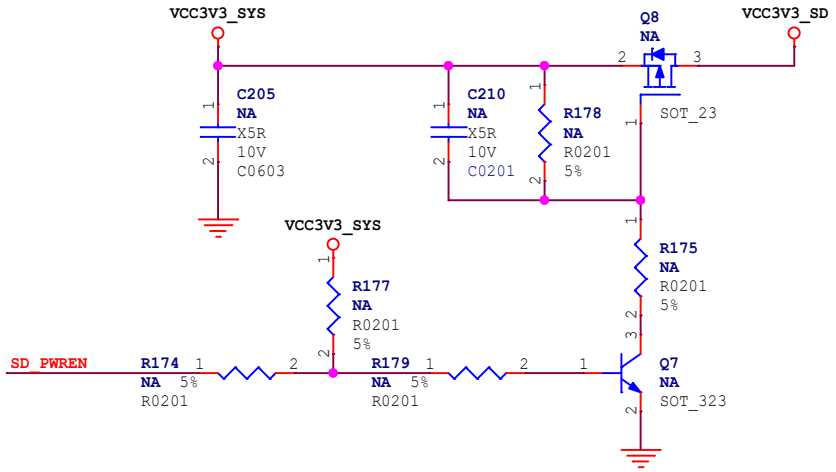
PCIe WIFI6/BT Module-2T2R



HINLINK			
Project:	**HNAS**		
File:	**24.PCIE_SDIO_WIFI**		
Date:	Thursday, November 30, 2023	**Rev:**	<Revision>
Designer:	<designer>	**Sheet:**	28 of 24



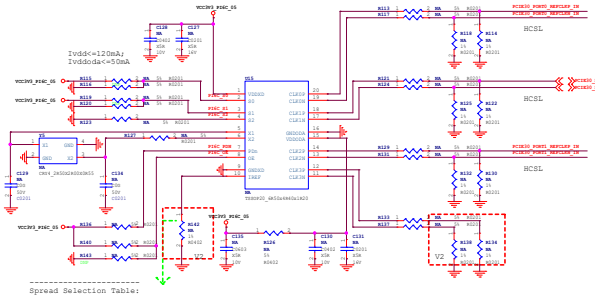
MicroSD Card



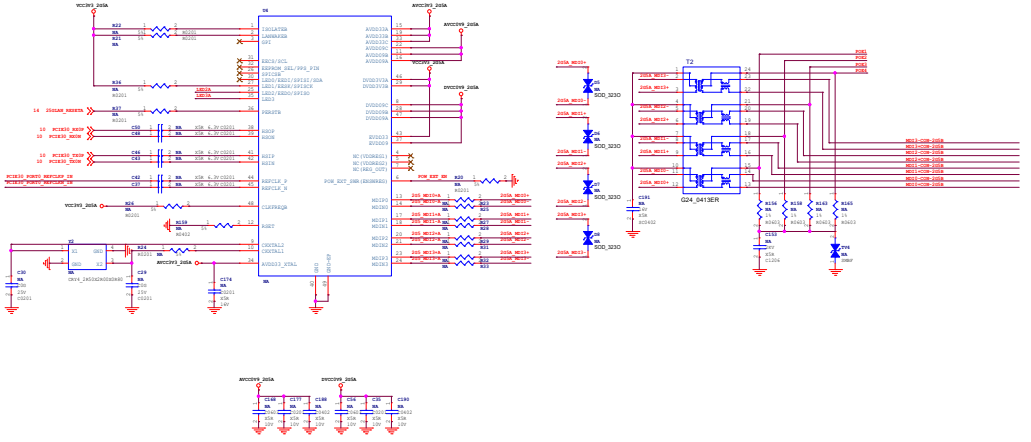
HINLINK			
Project:	HNAS	HINLINK	
File:	25.Flash-MicroSD Card		
Date:	Sunday, June 23, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 25

PCIE CLK

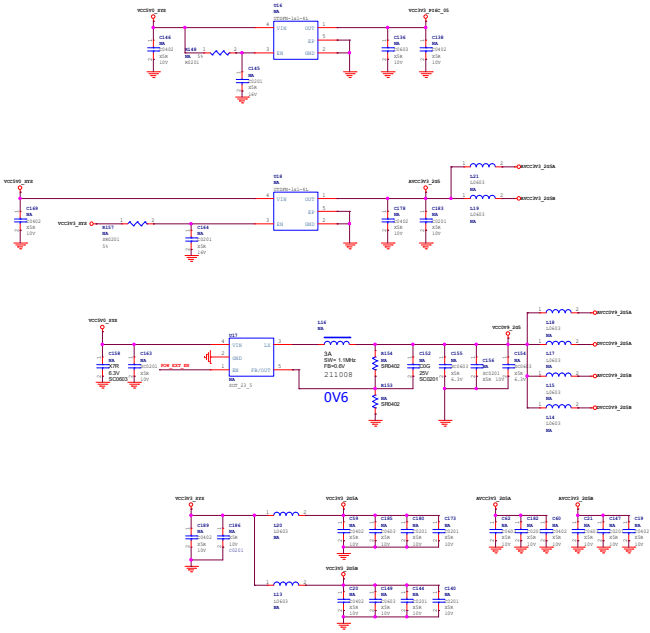
Crystal Generator



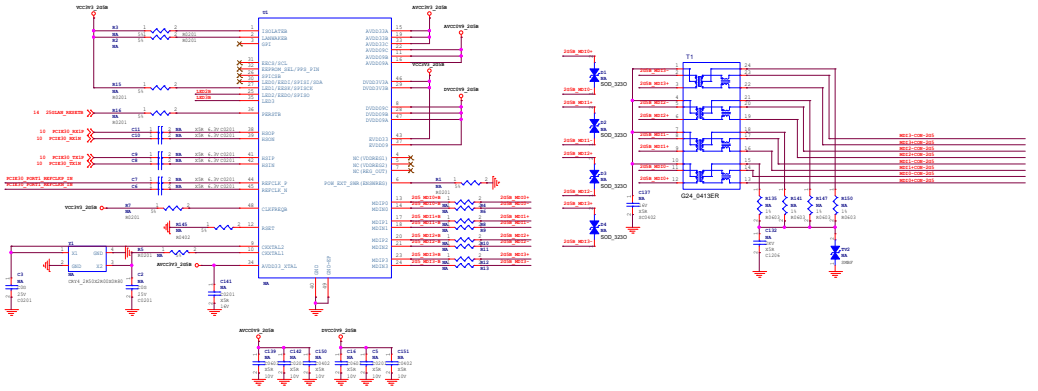
PCIE 2.5G A



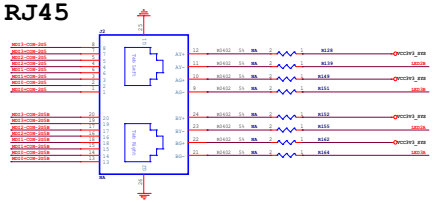
PCIE POWER

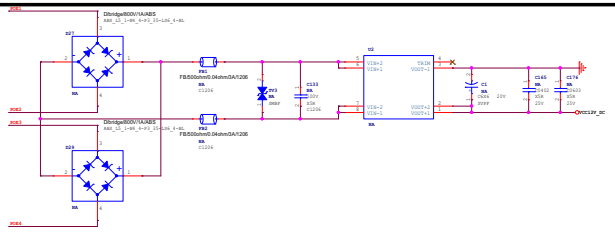


PCIE 2.5G B

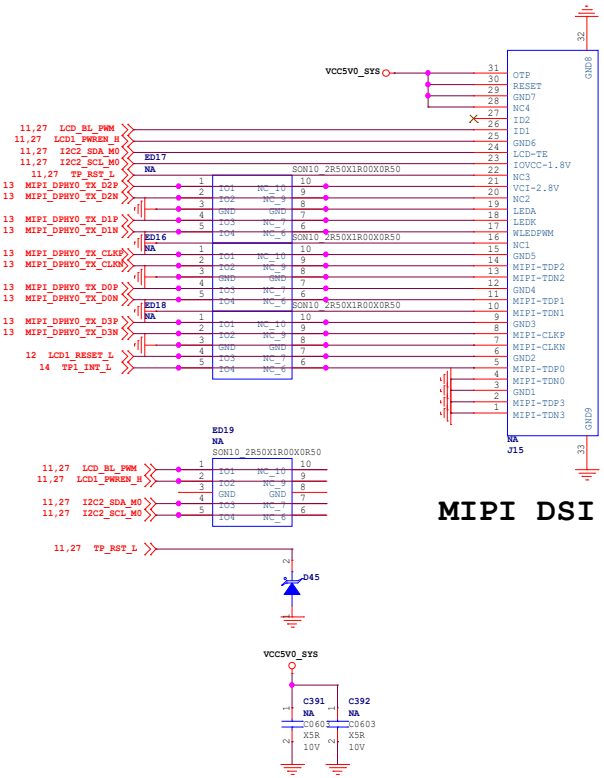


RJ45





HINLINK		
Project:	HNAS	
File:	20.204_ETH	
Date:	Tuesday, November 30, 2021	Rev:
Designer:	<designer>	Sheet: 20 of 20



MIPI DSI

HINLINK		
Project:	HNAS	HINLINK
File:	27.VO-LCM_MIPI	
Date:	Thursday, November 30, 2023	Rev. <Revision>
Designer:	<designer>	Sheet 28 of 27

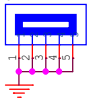
MARK2
NA

MARK1
NA

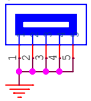
MARK6
NA

MARK5
NA

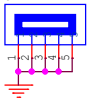
SHIELD1
NA
SHIELD-1



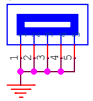
SHIELD2
NA
SHIELD-1



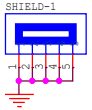
SHIELD4
NA
SHIELD-1



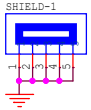
SHIELD6
NA
SHIELD-1



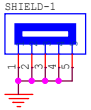
SHIELD8
NA
SHIELD-1



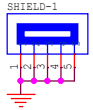
SHIELD7
NA
SHIELD-1



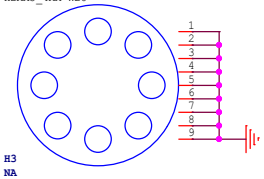
SHIELD5
NA
SHIELD-1



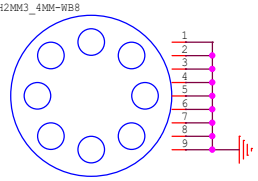
SHIELD3
NA
SHIELD-1



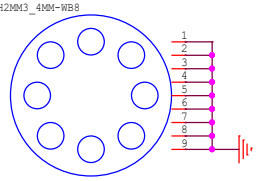
H1
NA
H2MM3_4MM-WB8

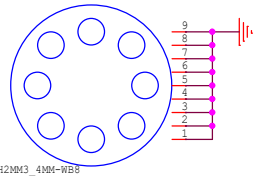


H2
NA
H2MM3_4MM-WB8



H3
NA
H2MM3_4MM-WB8





H2MM3_4MM-WB8
NA
H4

HINLINK		
Project:	HNAS	
File:	28.Mark/Hole/Heatsink	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 28